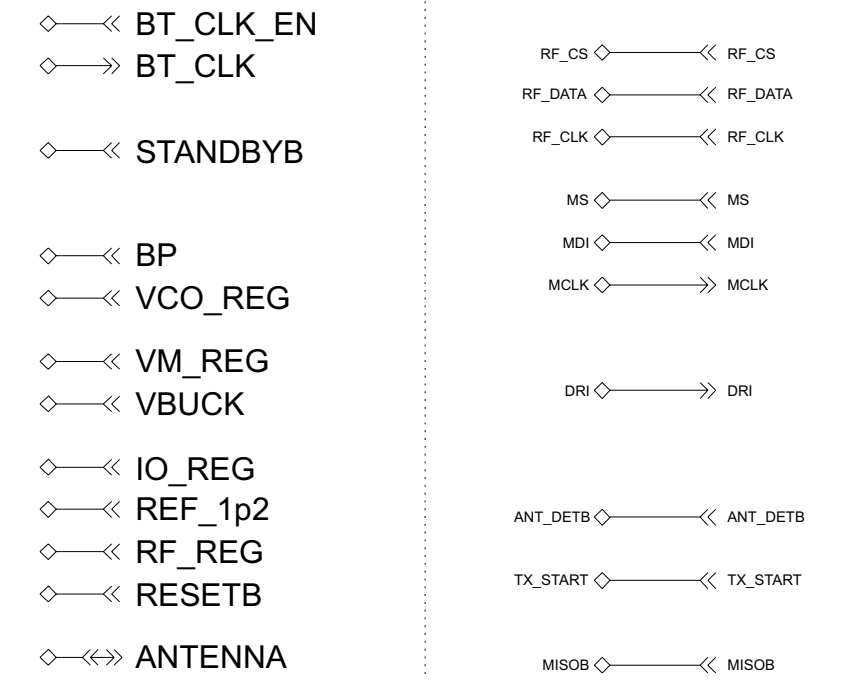
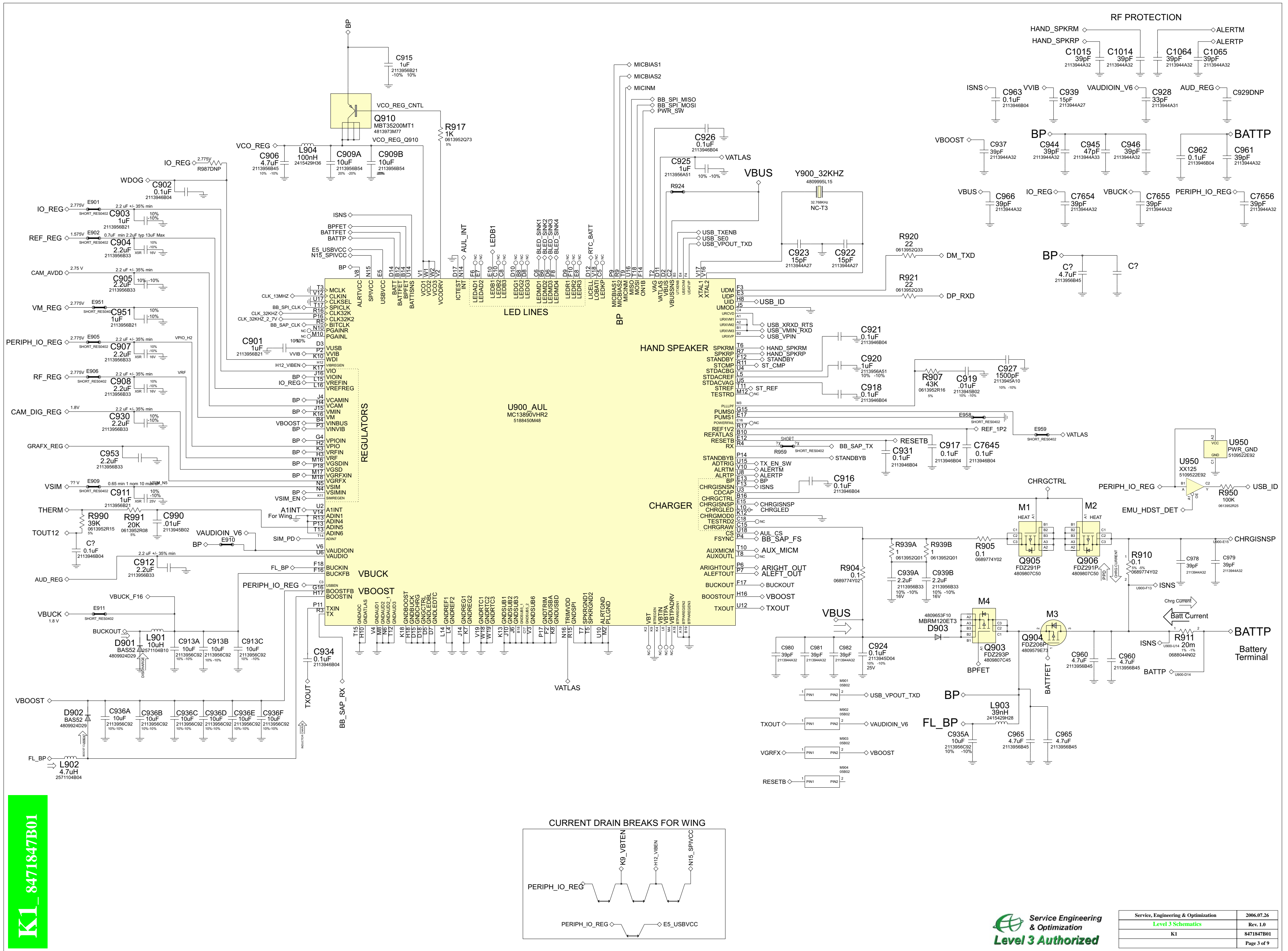
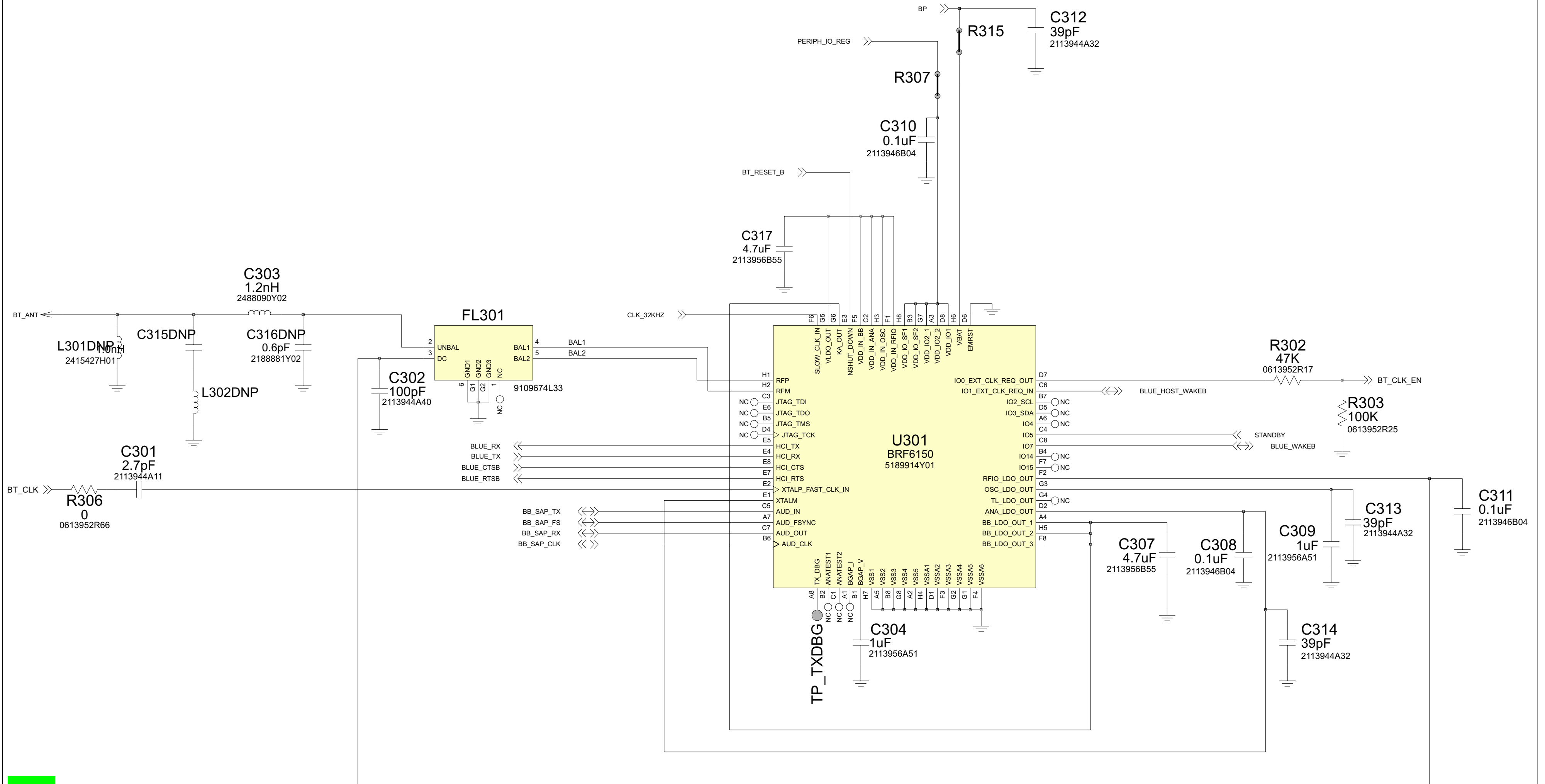


NEPTUNE INTERFACE

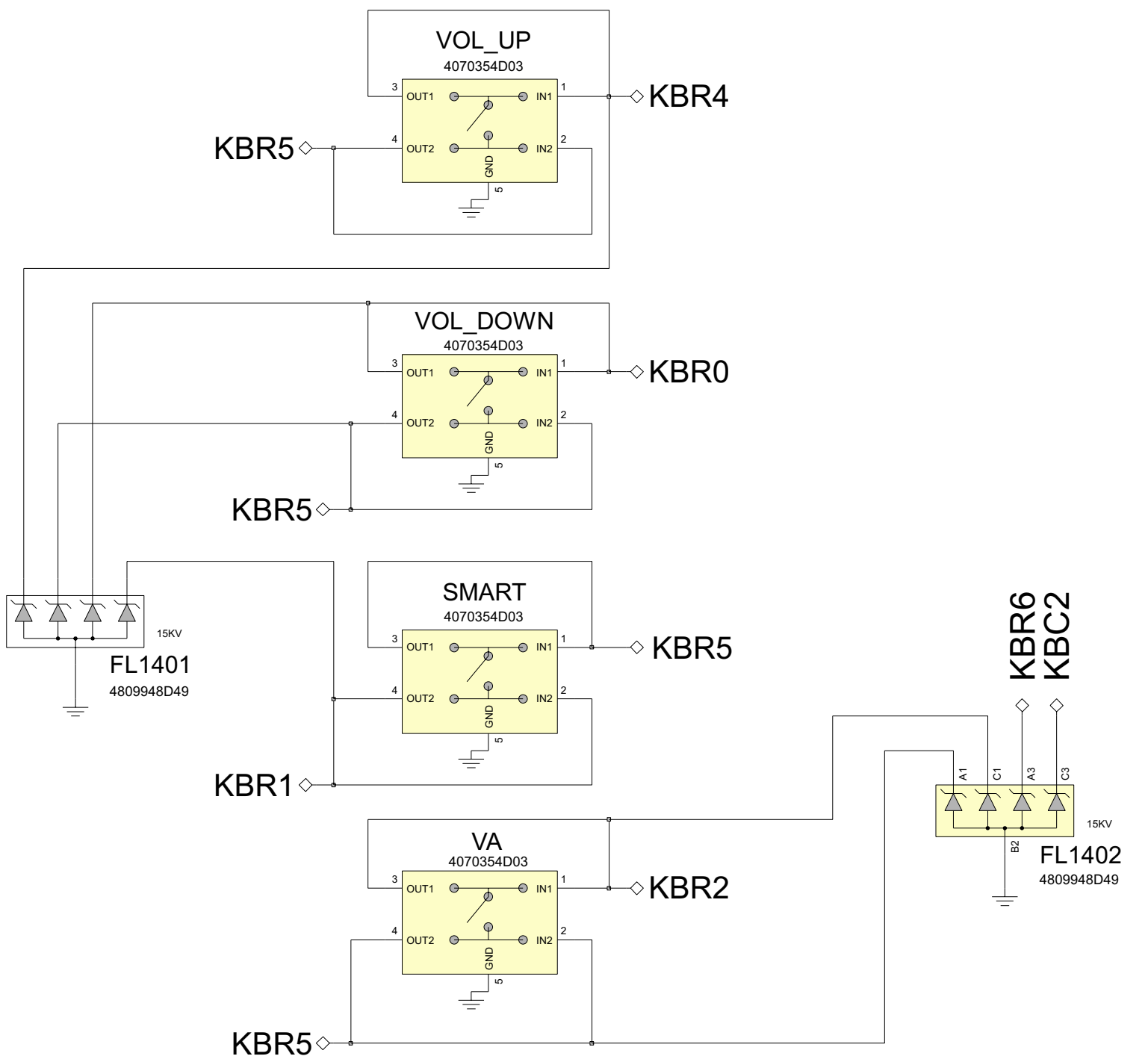




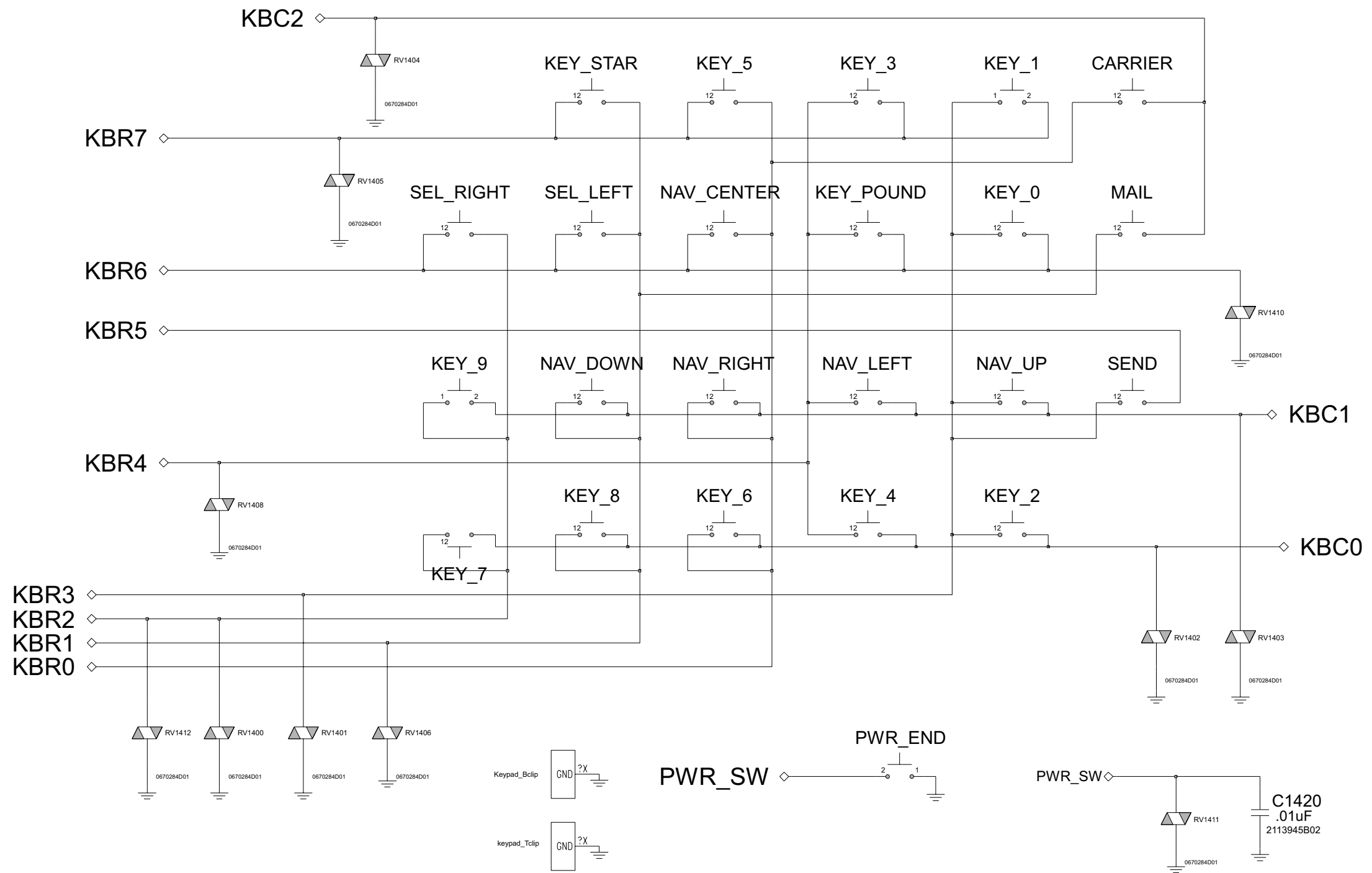




SIDEKEY SWITCHES

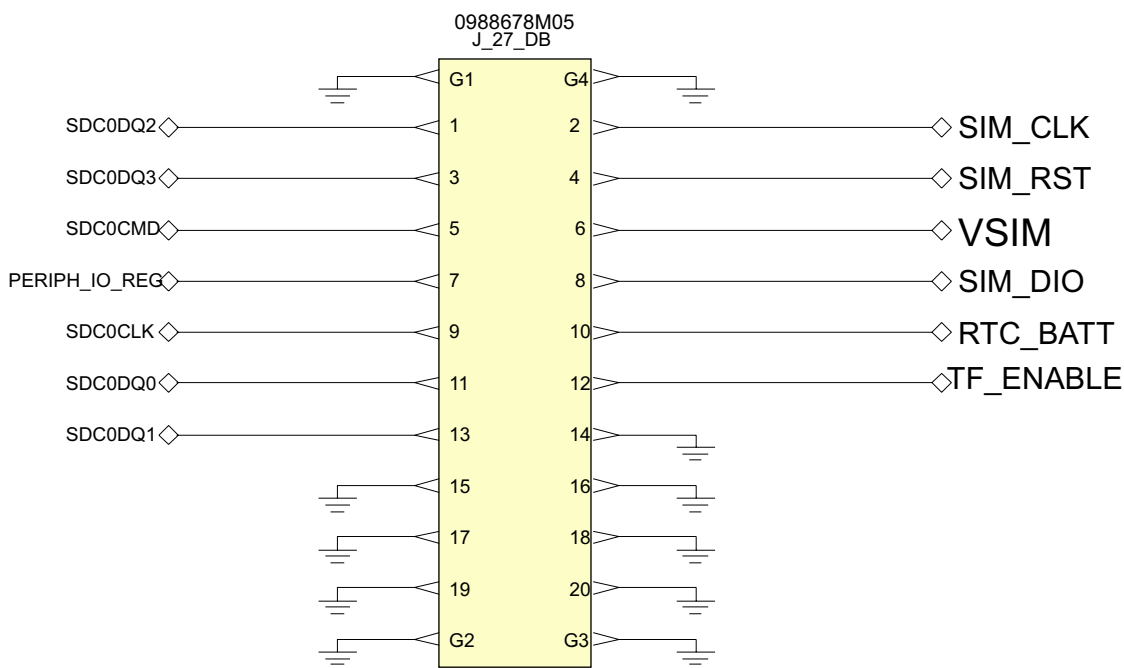
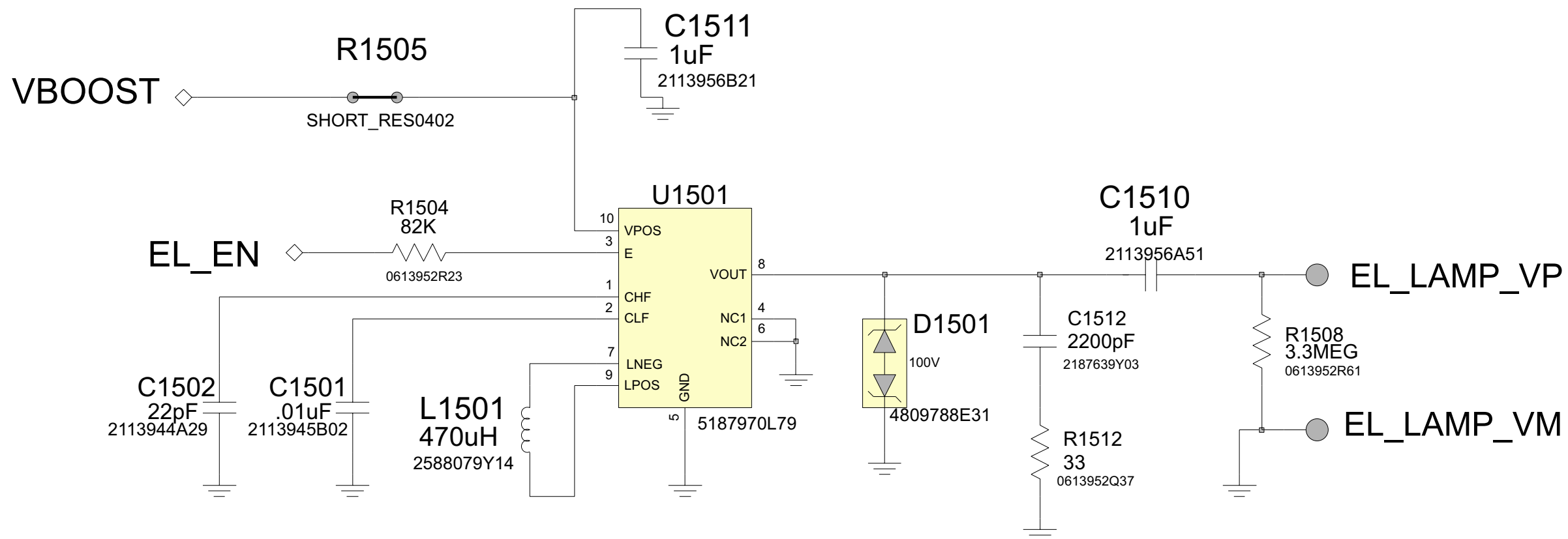


KEYPAD



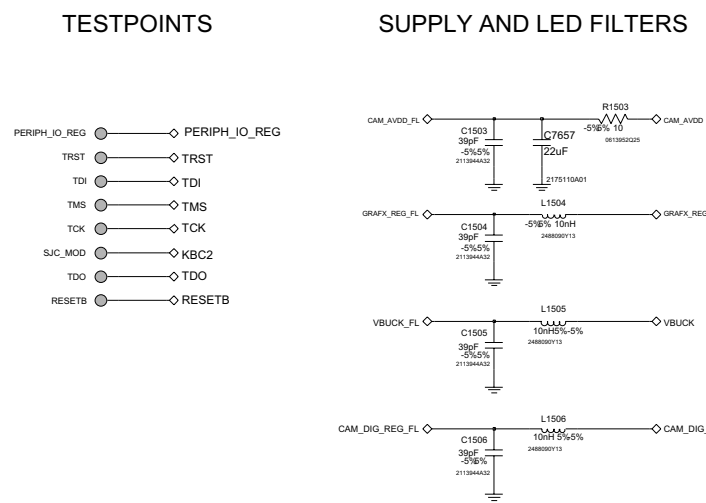
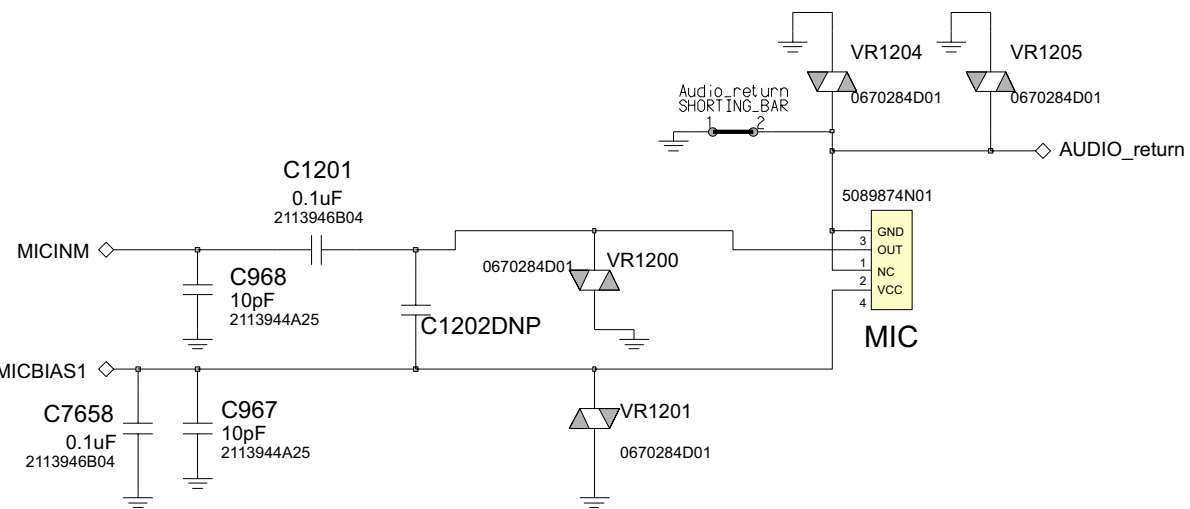
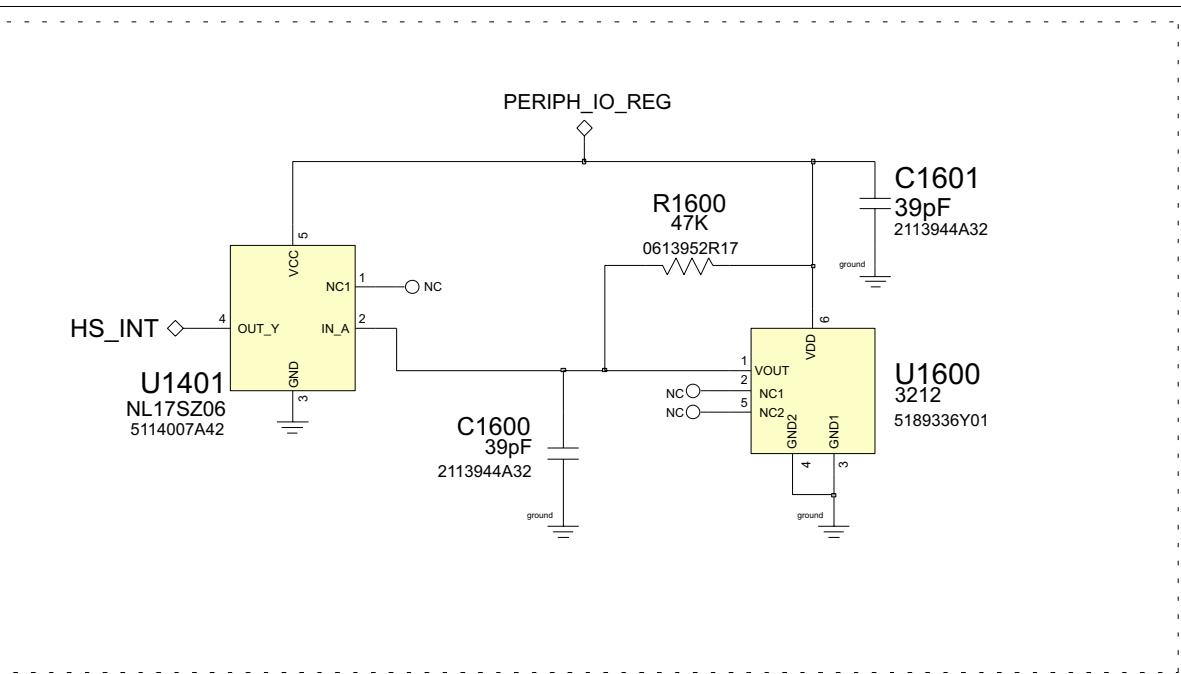
DAUGHTER BRD CONNECTOR

EL DRIVER



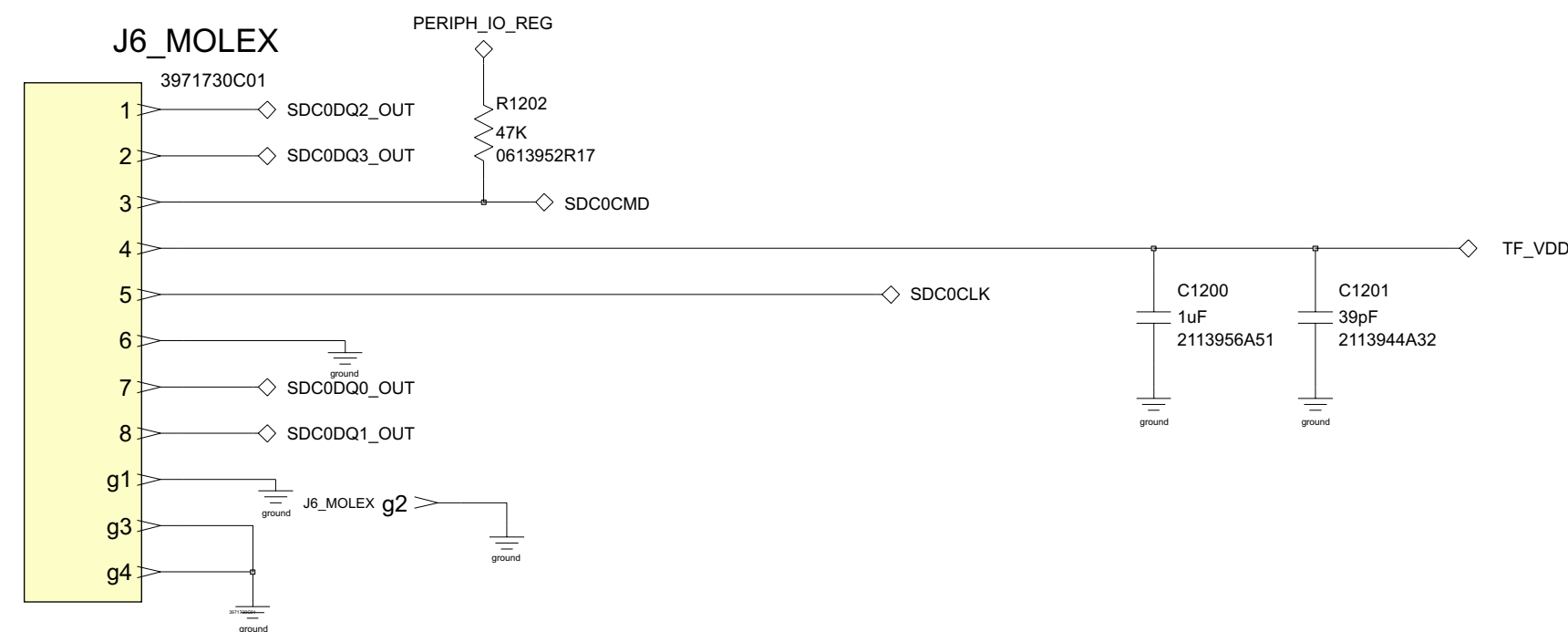
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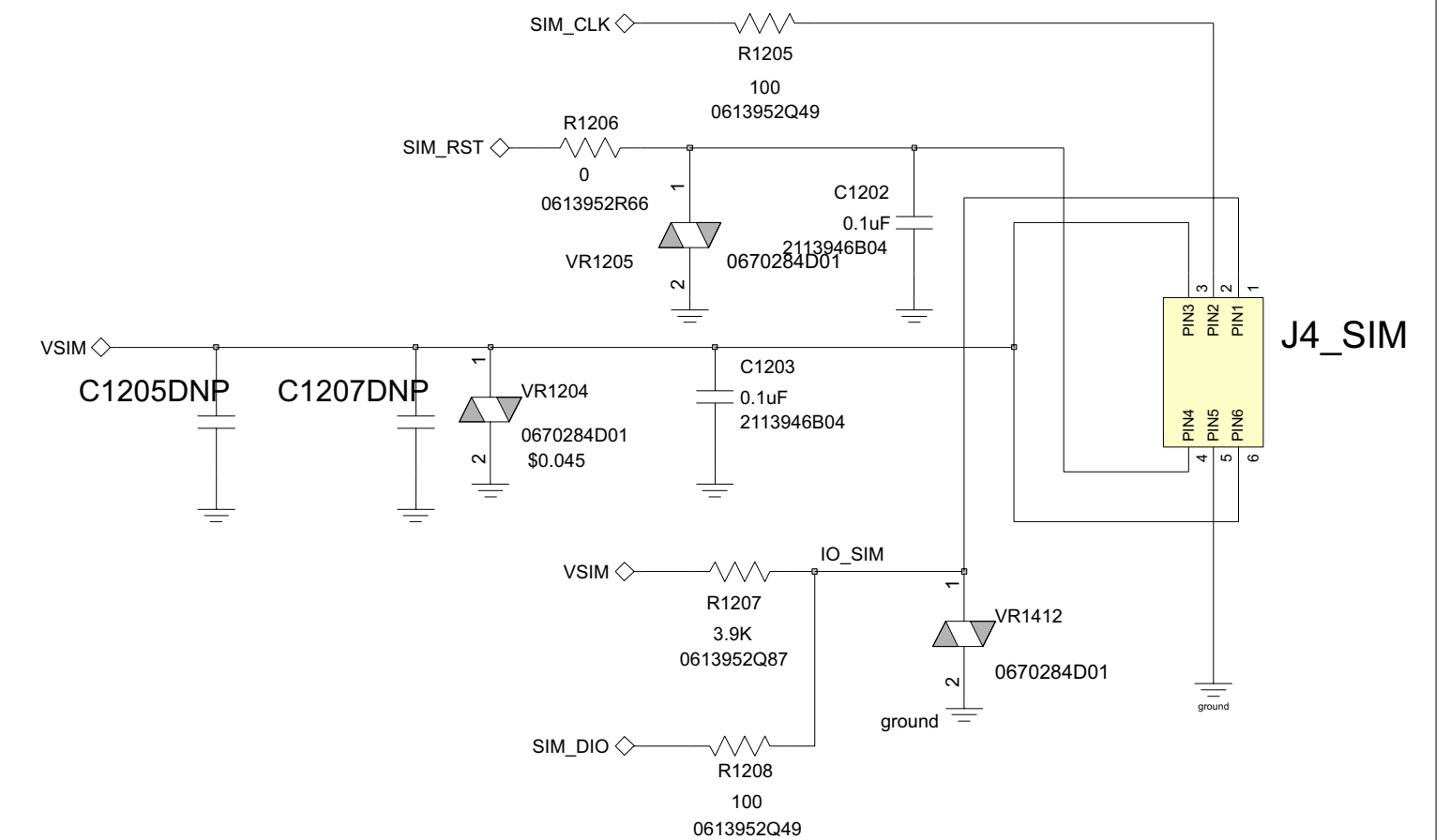


DAUGHTER BOARD SCHEMATIC

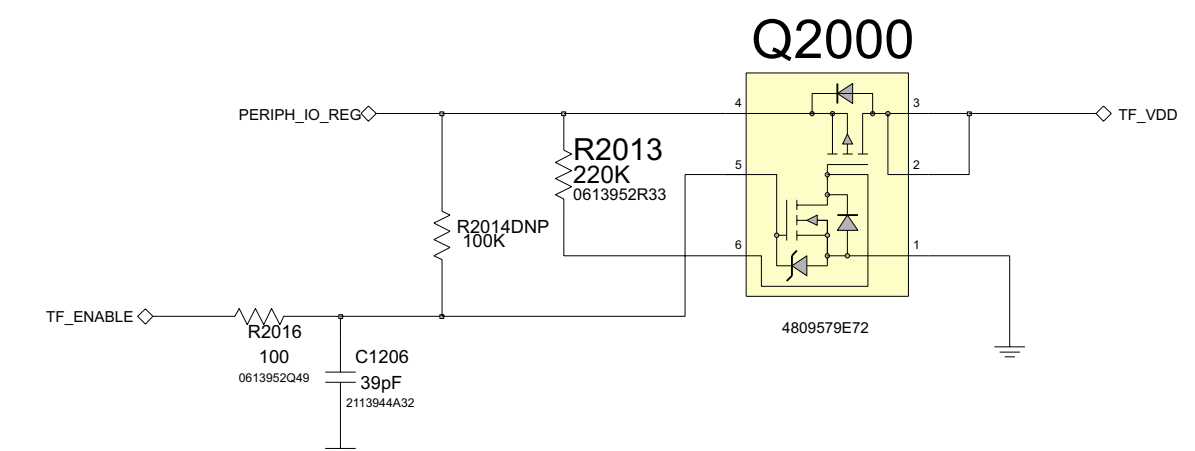
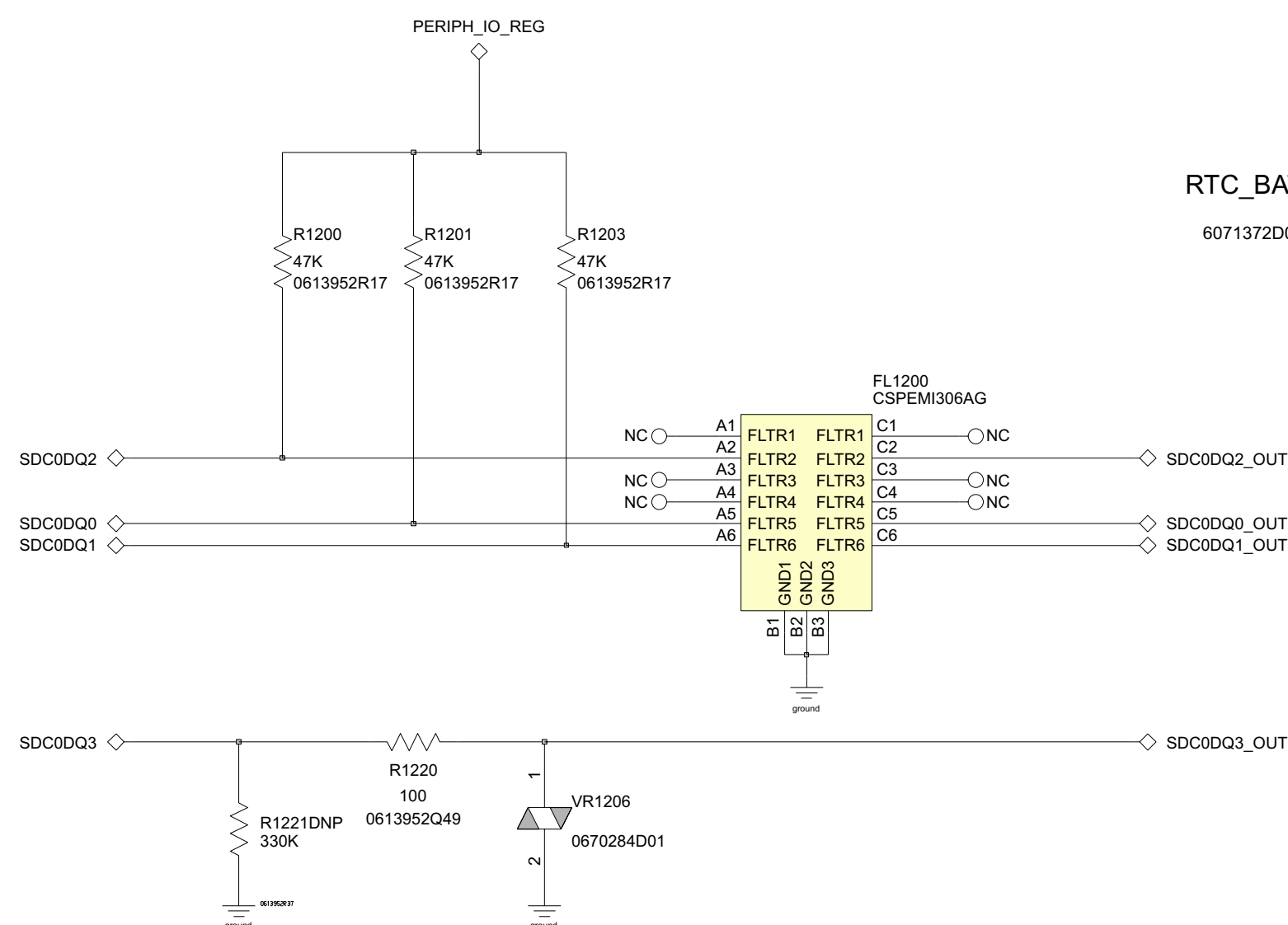
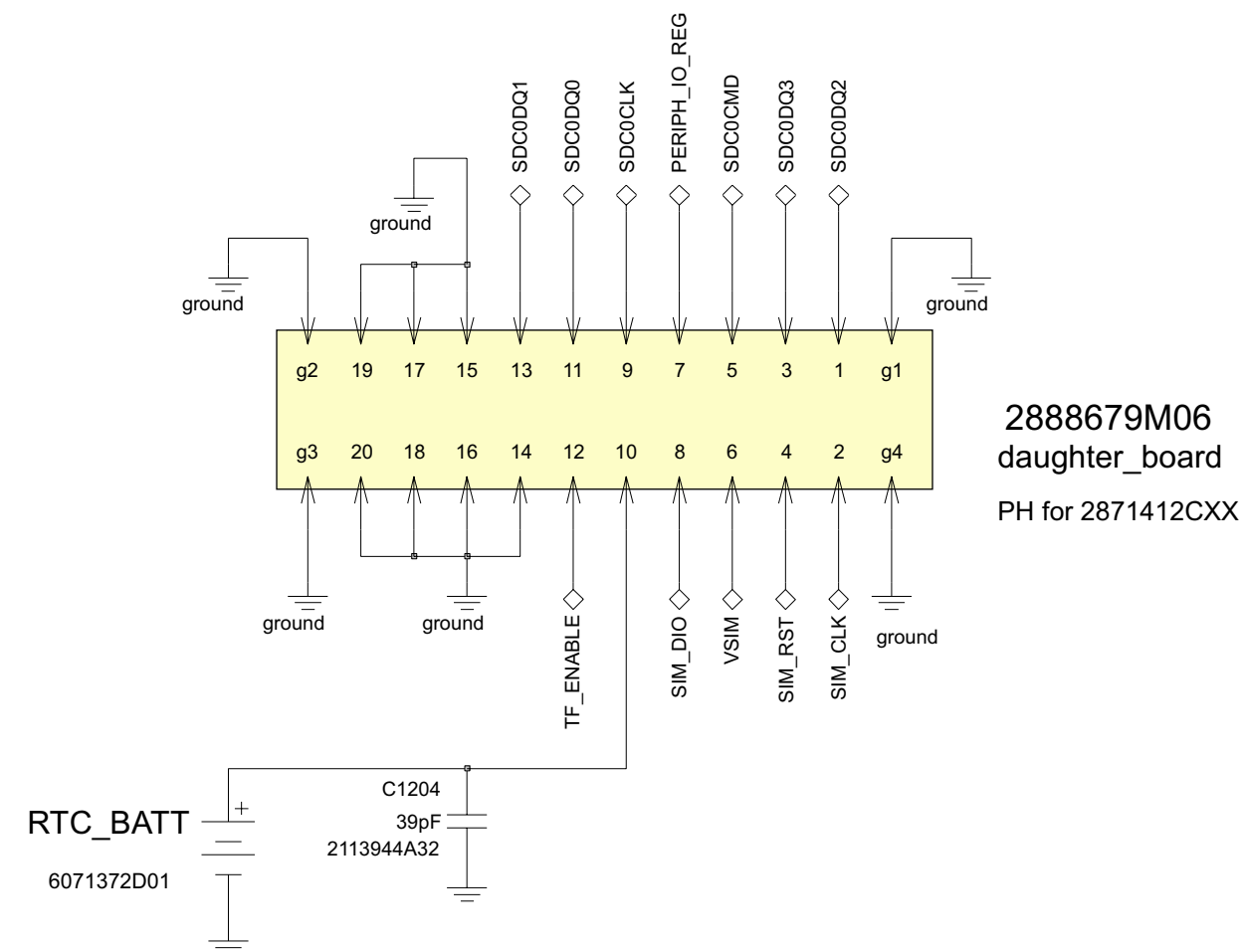
TRANSFLASH



SIM BLOCK

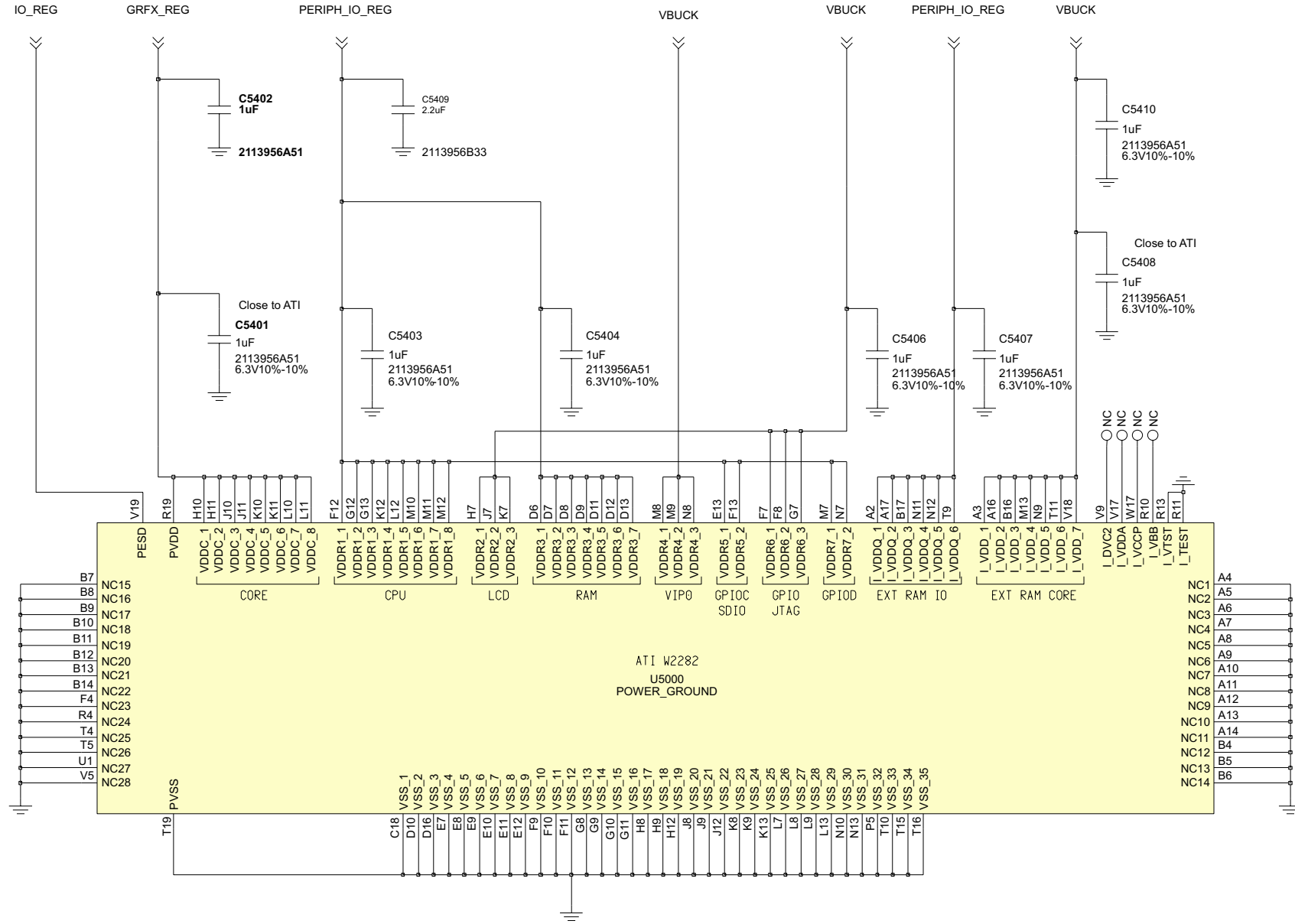


BOARD TO BOARD PLACEHOLDER



JK1_8471946B01_O

K1_8471501D01_A



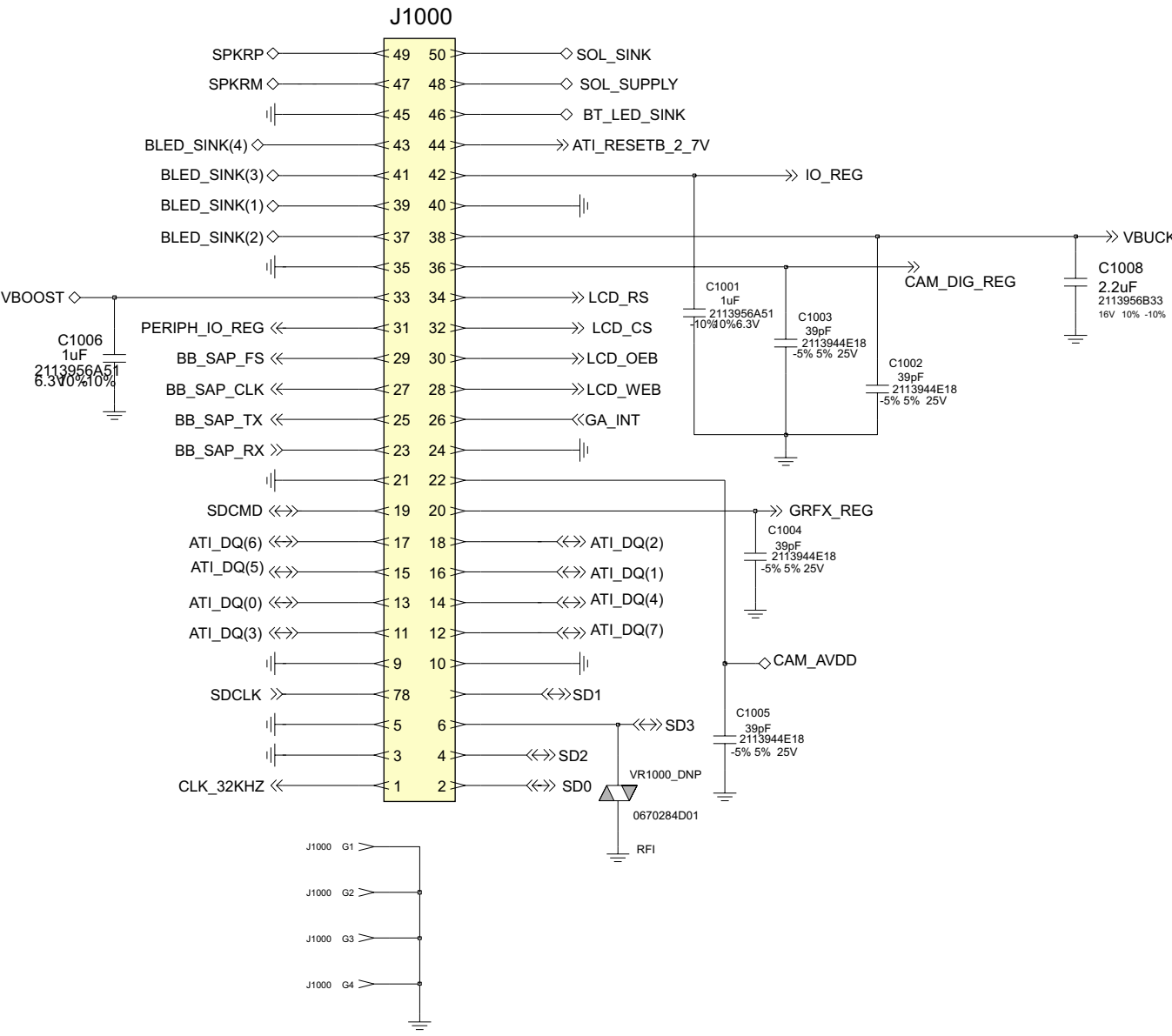
The diagram illustrates the AT1 W2282 camera module interface. The module is represented by a yellow block with various pins. On the left, there are connections for SDCLK (to SD1), SD3, and SDCMD. On the right, there are connections for CAM_PD and CAM_RST. The module has two main interfaces: a parallel interface (pins B2-E1) and a serial interface (pins W2-V4). The serial interface is labeled 'U5000 GPIO_SD_INTERFACE'. The parallel interface includes pins for LDCS, LDCS_SDO, LDCS_SCL, CLI_CS, LDCS_RESETB, CLI_SCLK, CLI_RS, and CLI_SDATA. The serial interface includes pins for BB_SAP_CLK, BB_SAP_FS, BB_SAP_TX, NC, BB_SAP_RX, and SD pins (SD0, SD1, SD2, SD3). The module is powered by VBLK and has a 5% tolerance resistor R5003 (10K) connected to CAM_PD. The module is labeled 'AT1 W2282' and 'U5000'.

The diagram illustrates the AT1 W2282 CPU interface. Key components and connections include:

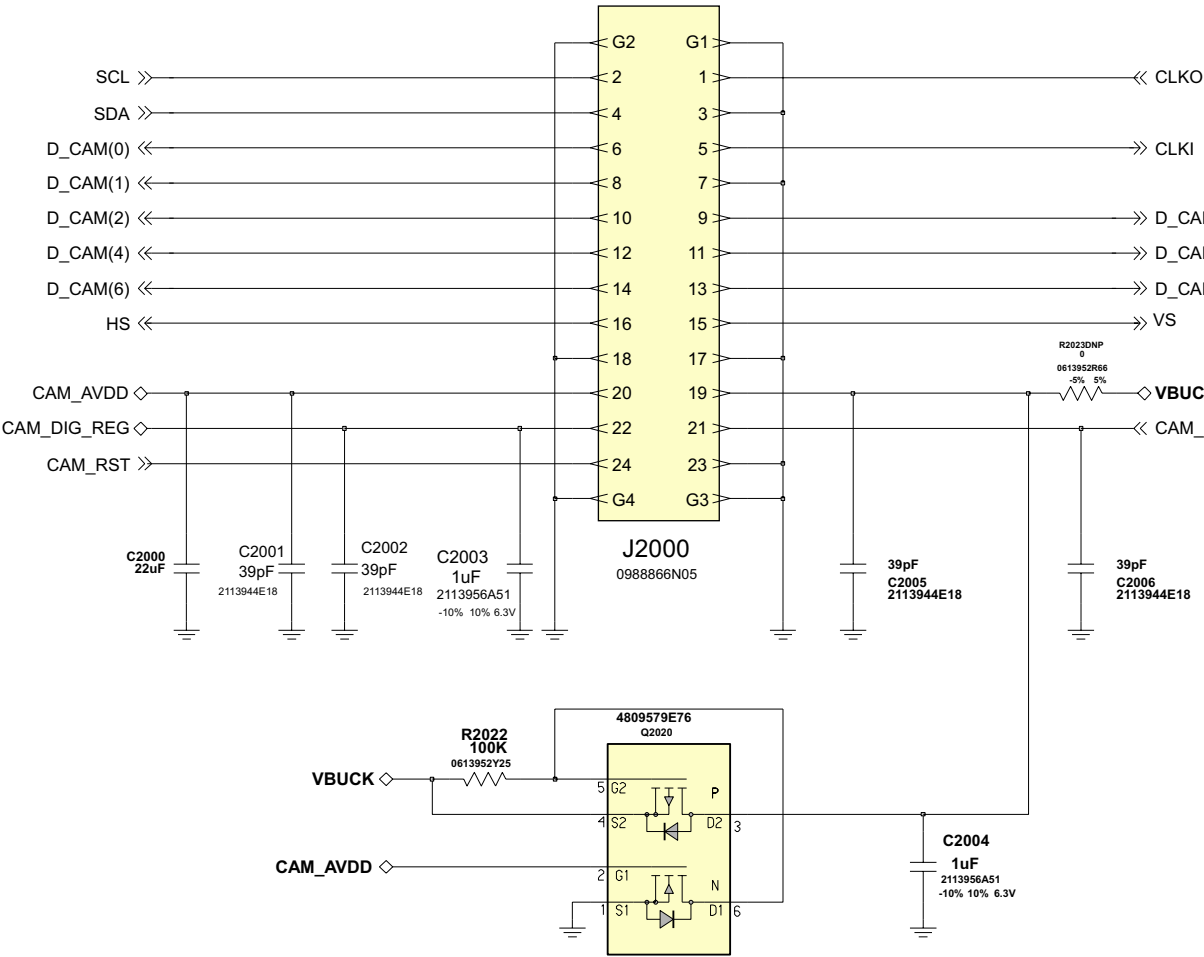
- AT1 W2282 CPU:** A central yellow block with pins for SRCLK, SLEEP, TESTEN, RESETB, and various data/address lines (DQ0-DQ15, AD0-AD17).
- External Components:**
 - U19:** SRCLK and SLEEP pins connected to CLK_32KHZ and AT1_RESETB_2_TV.
 - J1:** FS pin connected to ground.
 - C5200:** 1uF capacitor connected to ground.
 - VR5200:** Voltage detector connected to DQ0-DQ15 and AD0-AD17.
 - 4809948D48:** Component connected to DQ0-DQ15 and AD0-AD17.
- Signal Lines:**
 - CLK_32KHZ:** Connected to U19 SRCLK.
 - AT1_RESETB_2_TV:** Connected to H16 RESETB.
 - GA_INT:** Signal line connected to INT0B (E14 NC) and INT1B (G15 NC).
 - LCD_RS:** Connected to P15 AD0.
 - LCD_CS:** Connected to M19.
 - LCD_OEB:** Connected to N19.
- Other Connections:**
 - WAITB:** Connected to G16 NC.
 - IO_REG:** Connected to P16 AD22.
 - MR:** Connected to N16.
 - BE0, BE1:** Connected to F19 and G19.
 - CSB:** Connected to M19.
 - WEB:** Connected to P19.
 - OEB:** Connected to N19.

The diagram illustrates the camera interface circuit for the U5000 camera module. The camera module is represented by a yellow block labeled 'U5000 CAMERA_INTERFACE' with pins W5 through W9. The system's power and signal lines are represented by a white block labeled 'SYSTEM' with pins W6 through W9. The circuit includes a pull-up resistor R5005 (2.2K, 5%) connected to VBUCK and the SCL line, and a pull-down resistor R5006 (2.2K, 5%) connected to the SDA line. A 39pF capacitor C5301 is connected to the SDA line. The SCL line is connected to the RFI pin of the L5300 component. The SDA line is connected to the CLK pin of the L5300 component. The SCL line is also connected to the CLK pin of the L5300 component. The SDA line is also connected to the CLK pin of the L5300 component.

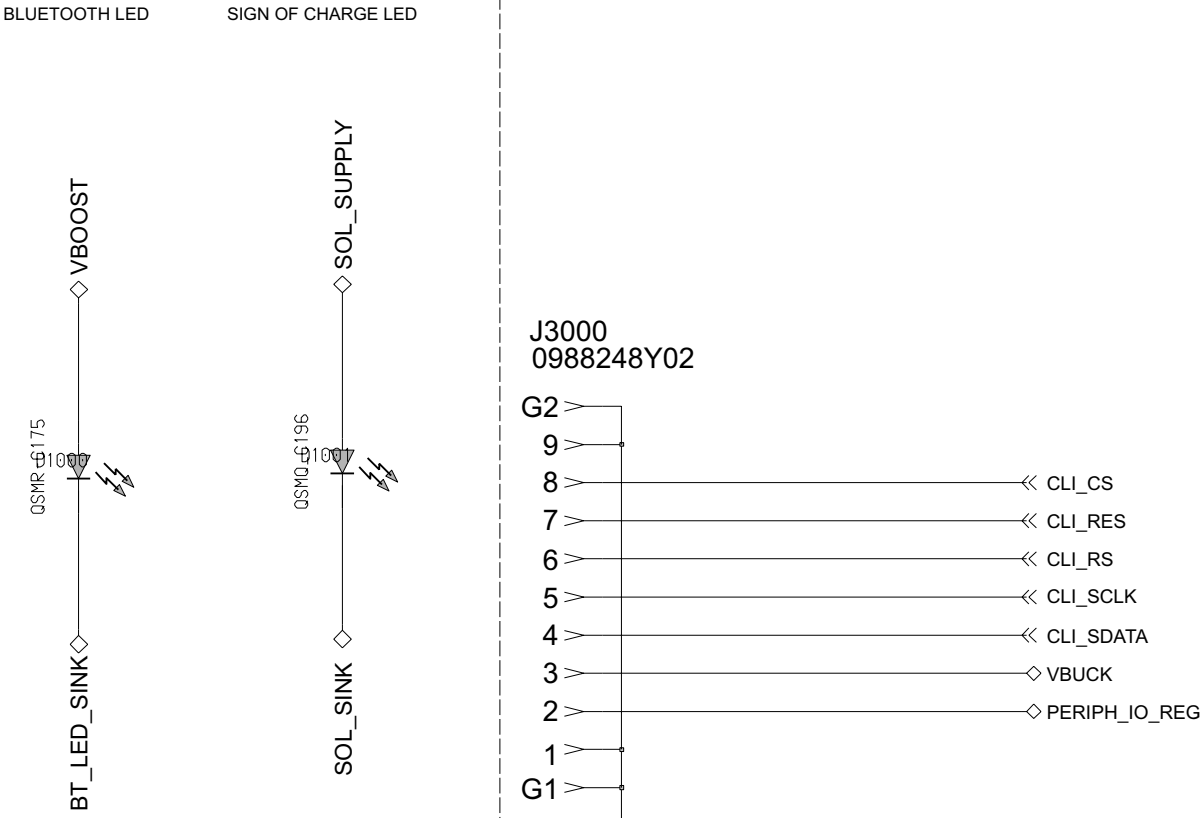
50 PIN DISPLAY TO TCVR CONNECTOR



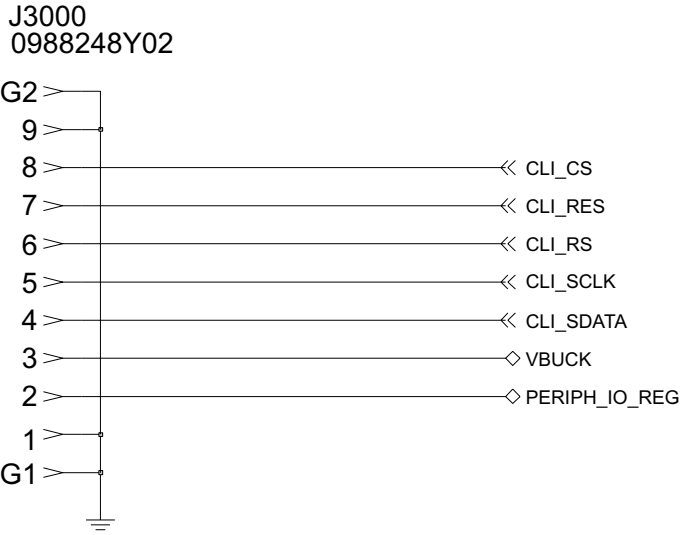
24-PIN TO CAMERA



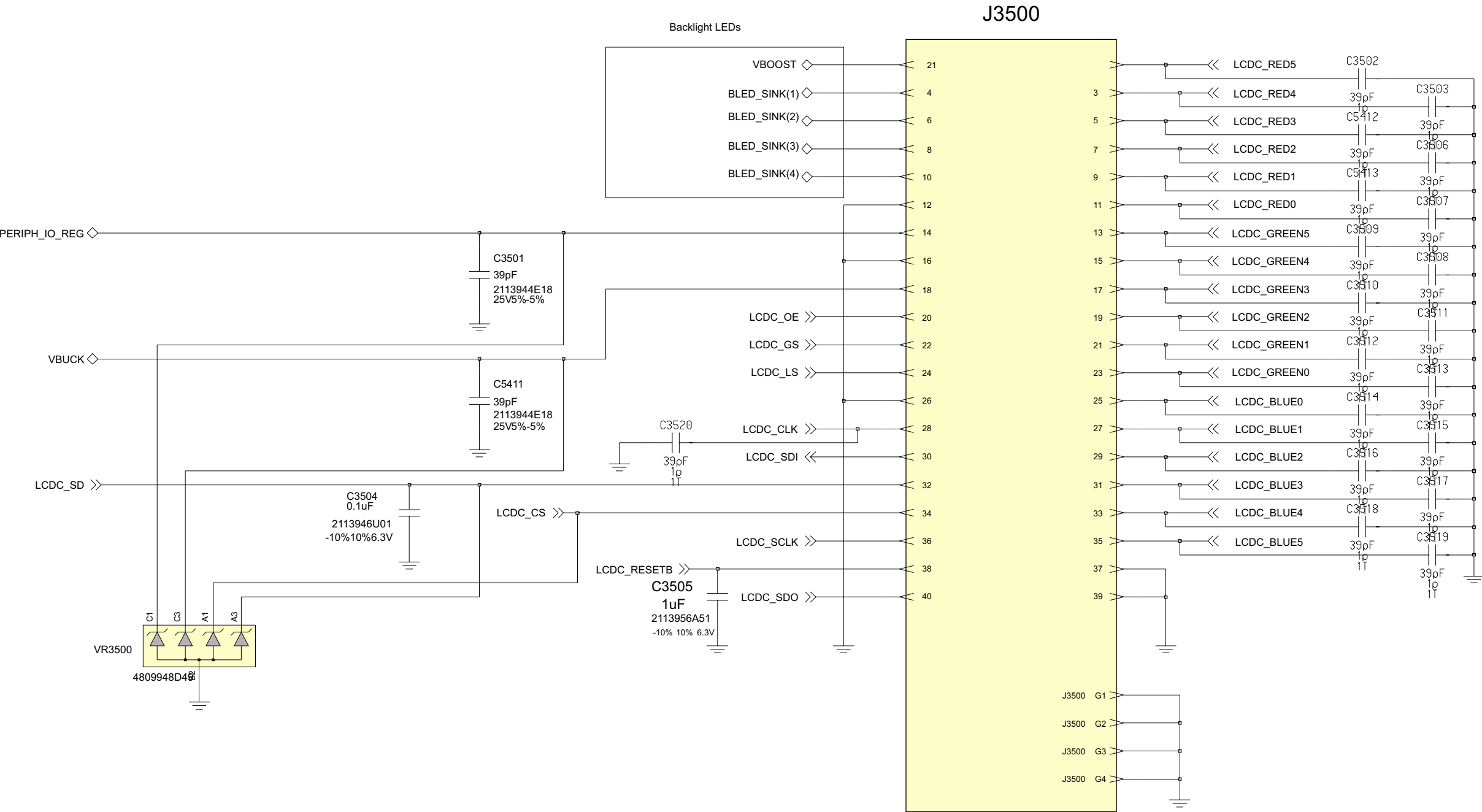
LEDS



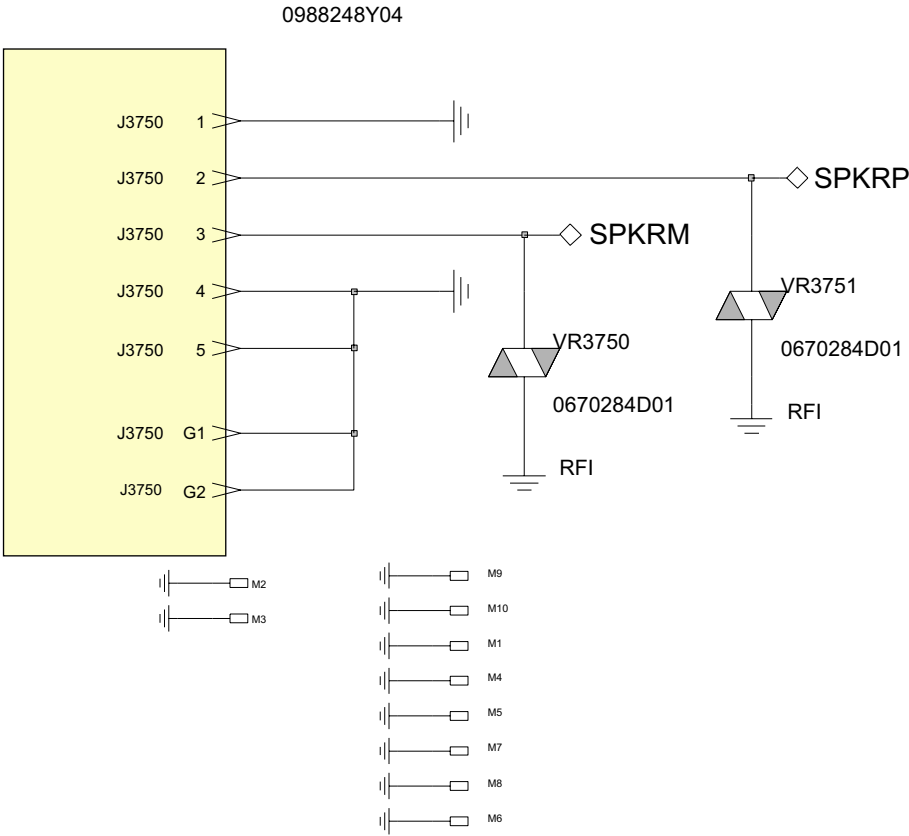
9-PIN CLI CONNECTOR



40-PIN MAIN DISPLAY



EAR SPEAKER



K1_8471501D01_A