Service Manual Level III

Motorola V60i

CDMA 800/1900/AMPS 800

FREQUENCY SYNTHESIZER CIRCUITRY

The phone contains three PLL frequency synthesizers controlled by U700.

1. The main VCO: there are two main VCO modules- a) one synthesizer controls the tunable 979 – 1004Mhz main local oscillator – U626, which is ON during Cellular or 800Mhz mode. b) another synthesizer controls the tunable 2039-2100Mhz main local oscillator – U636, which is ON during PCS or 1900Mhz mode.
2. The Tx offset VCO: there are two modes and two frequency at which this oscillator which is internal to U700 works, but the tank circuit is external. There are two tank circuits one for Cellular mode (800 Mhz) which will set 309.6Mhz frequency for the oscillator to oscillate on. Another tank circuit for PCS mode (1900Mhz) which will set 379.6Mhz frequency for the oscillator to oscillate on. The Tx offset frequency is divided by 2 before being fed into the mixer for modulation.
3. The second LO: the second local oscillator also operates in two modes with two different frequencies: For AMPS mode the frequency is 219.3Mhz and for CDMA mode at cellular or 800Mhz band and PCS or 1900Mhz band the frequency is 219.8Mhz. The tank circuit is external to the U700. The frequency is divided by 2 before being fed into the mixer.

All the synthesizers obtain their reference frequency from the 16.8Mhz reference oscillator.

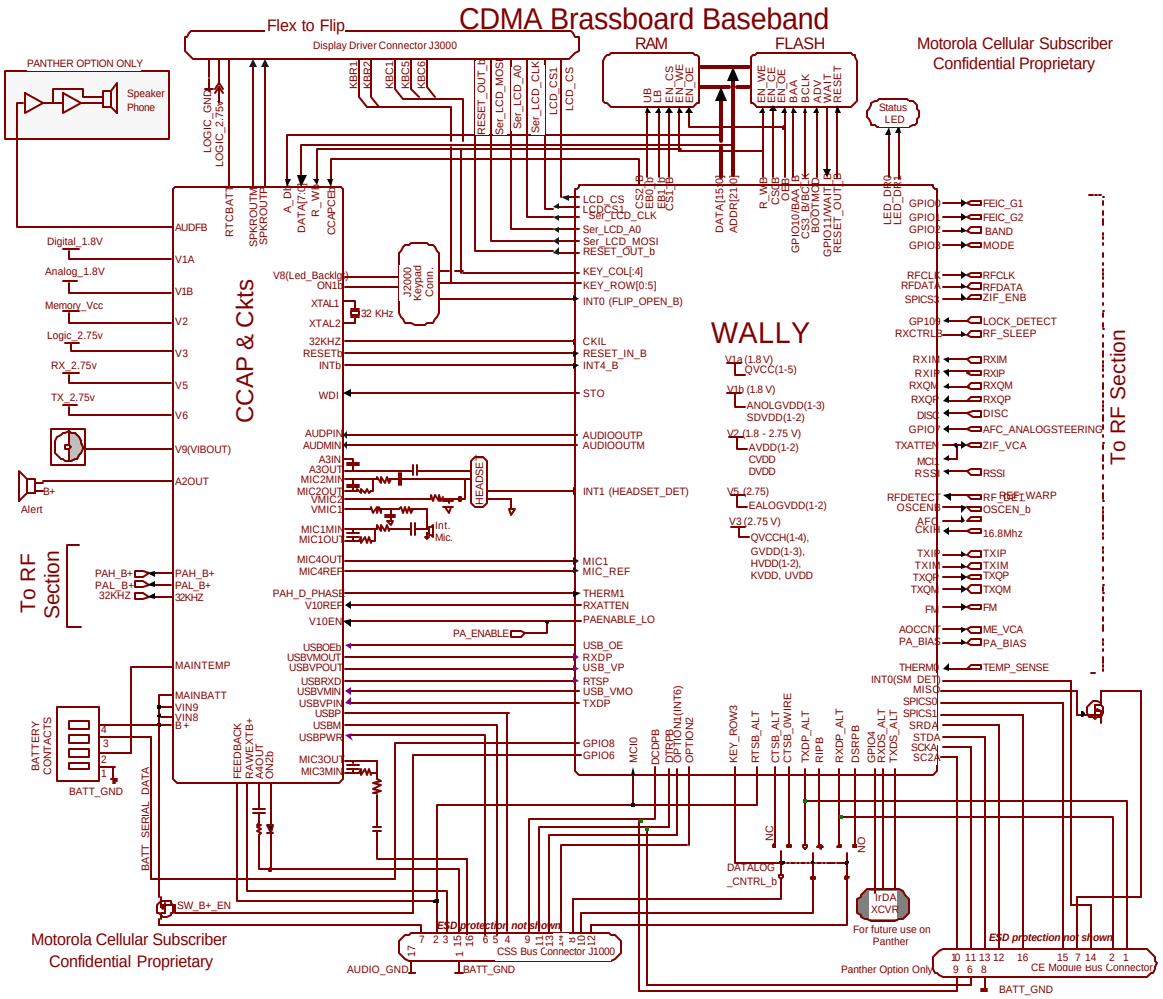
TRANSMIT POWER CONTROL CIRCUITRY

The transmit signal power (the output RF power) is controlled by the three control signals ZIF_VCA and ME_VCA from WALLY IC and PA_BIAS from CCAP IC. The output power is controlled at three places, ZIFSYN – U700 which has a gain control of max 40dB and ME3 IC- U400 which has a total gain of max 36dB and PA has a gain of max 27-32dB.

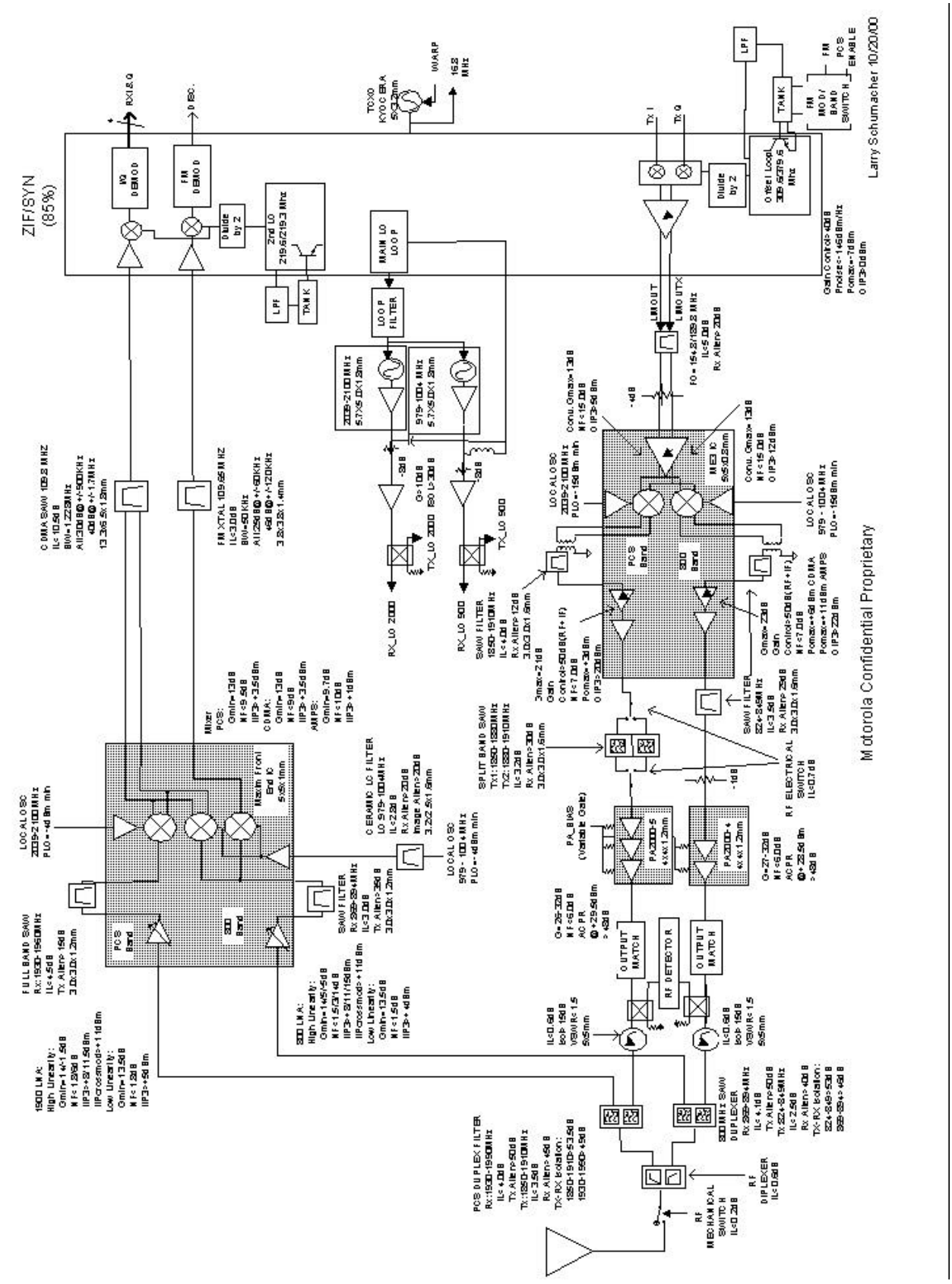
In Amps mode the power range is +8dBM to +28dBM. In CDMA mode the RF power range is from –50dBM to +23dBM.

In CDMA mode the power control operates in two mode: Open loop and Close loop. In open loop mode (at the beginning of registering – access probe) the power level is proportional to the received signal level, in close loop mode the power level is controlled by the CDMA cell based on the received signal strength at the cell site.

AUDIO LOGIC BLOCK DIAGRAM



RF SIDE BLOCK DIAGRAM



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ANTENNA CIRCUIT

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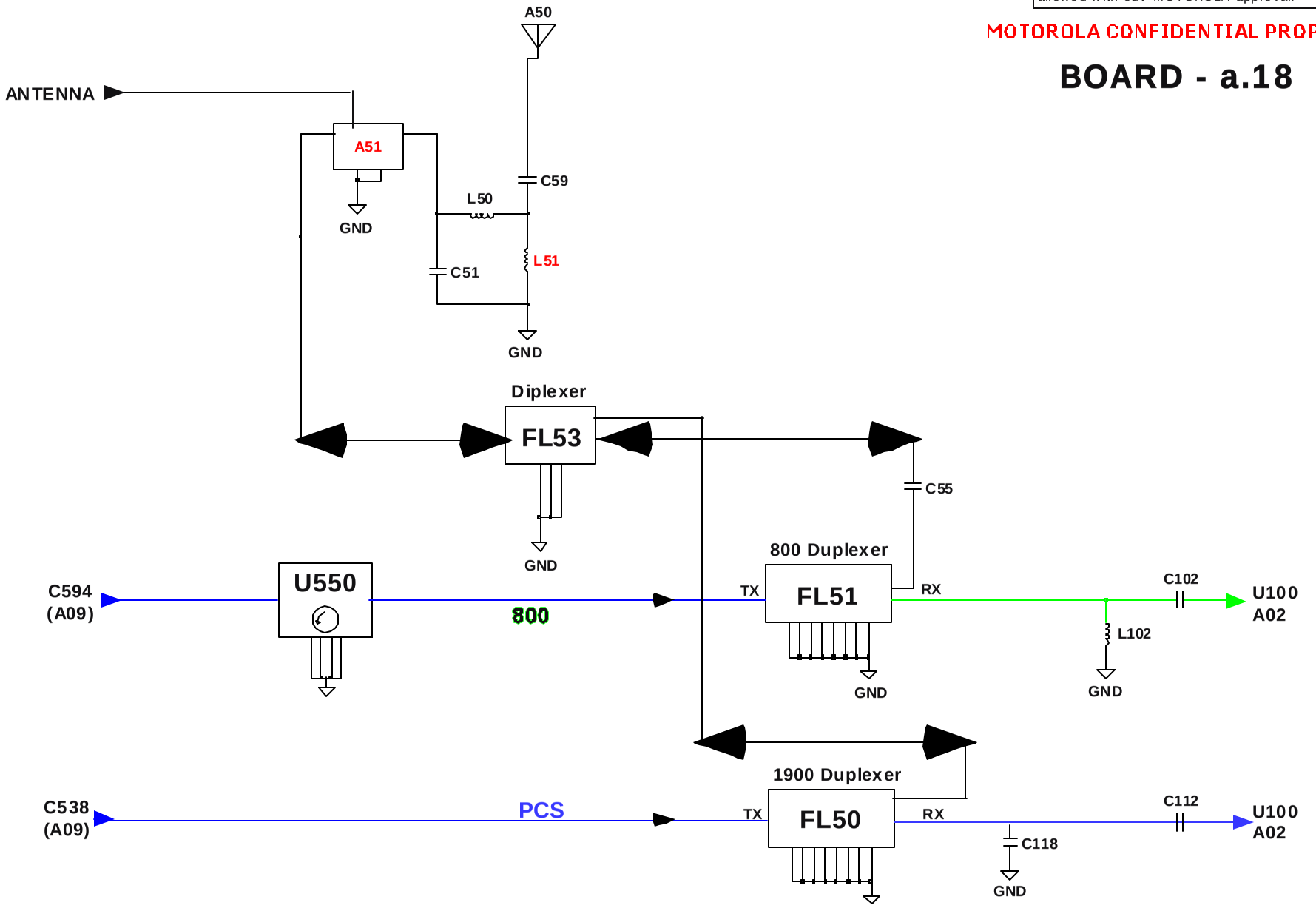

Antenna:A01

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FEIC CIRCUIT

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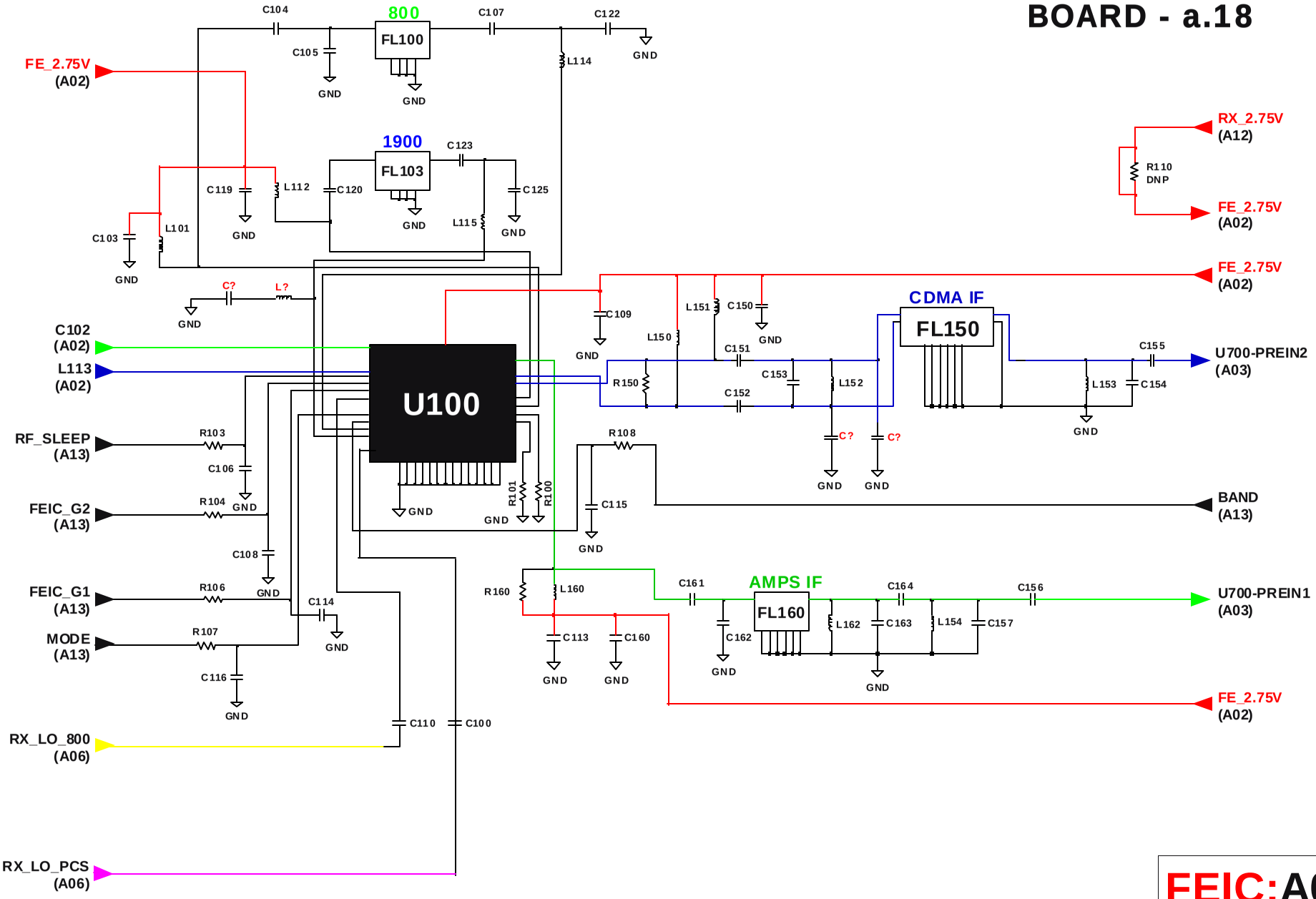

FEIC:A02

ZIF/SYN CIRCUIT

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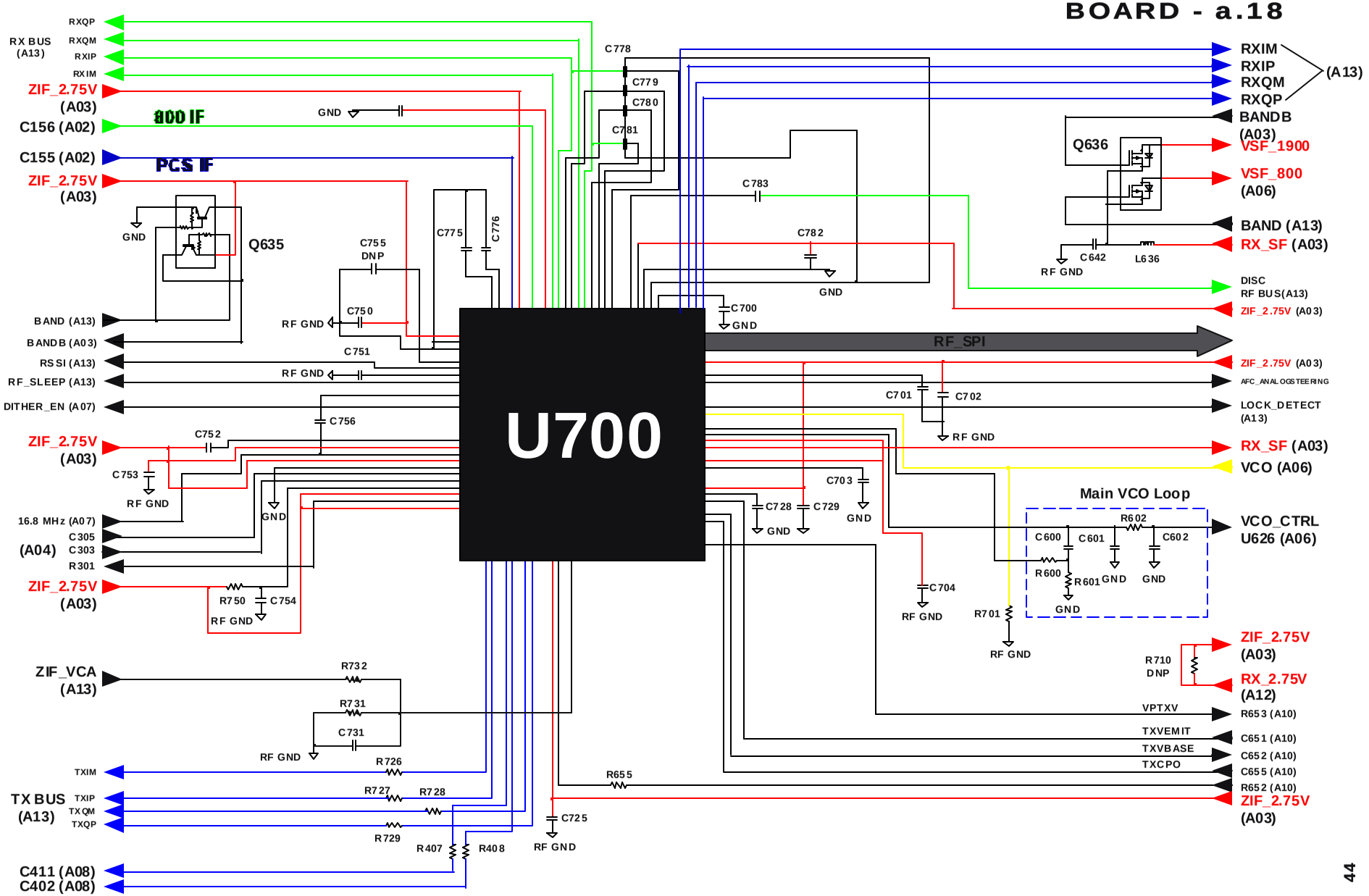

ZIF:A03

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2nd LO Circuit

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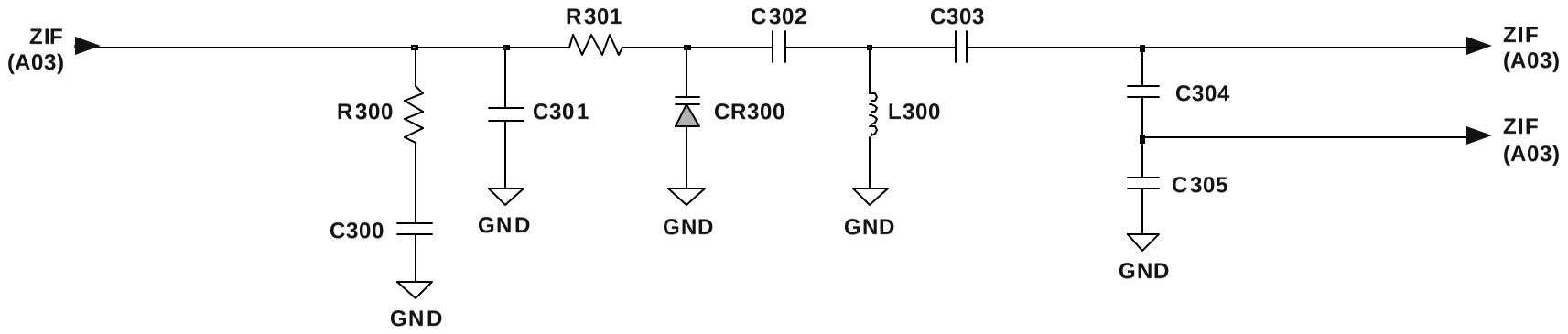

RX 2nd LO: A04

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TX OFFset Circuit

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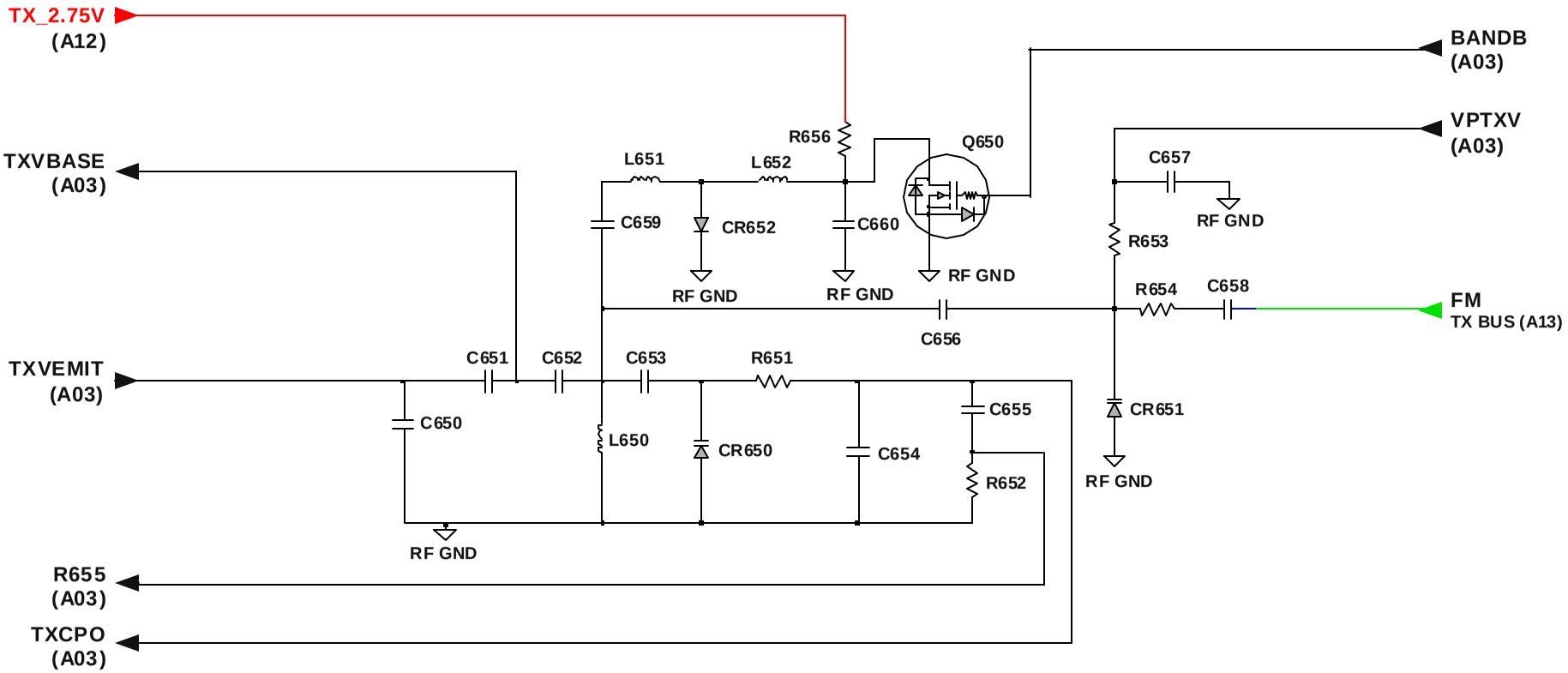

TX Offset Osc: A05

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VCO Circuit

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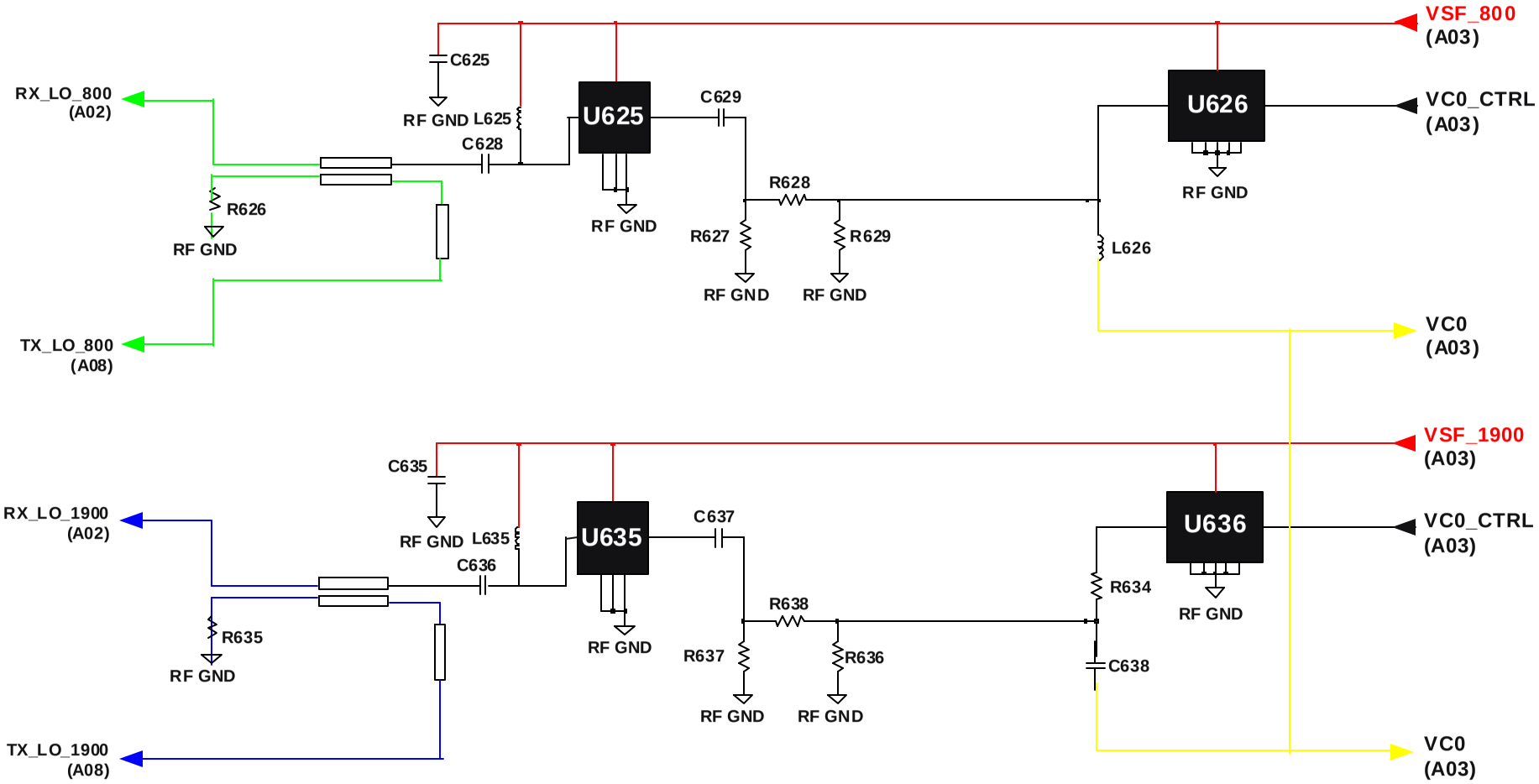

VCO:A06

V60i

REFERENCE OSCILATOR

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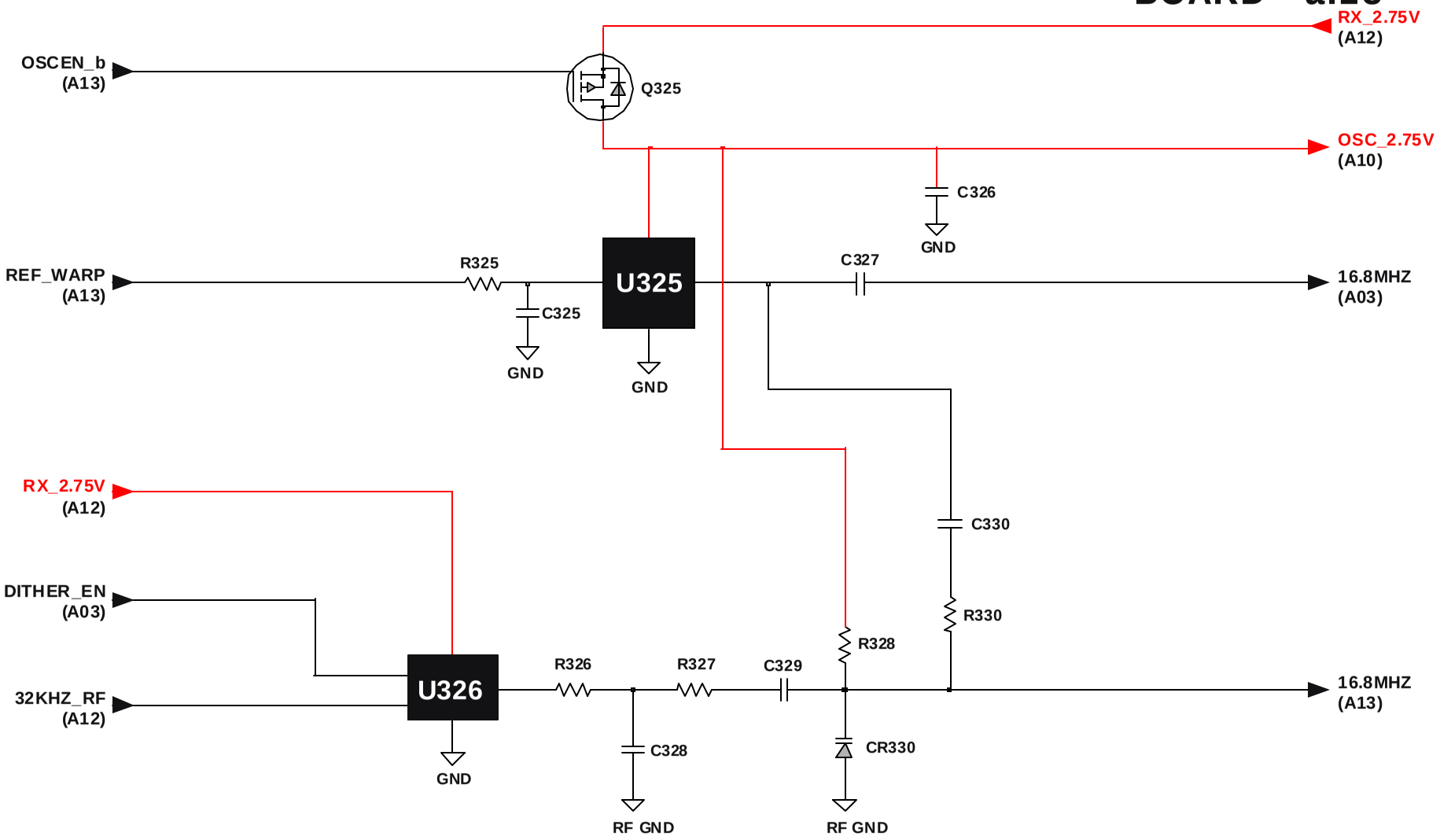

Ref Osc: A07

ME3 Circuit

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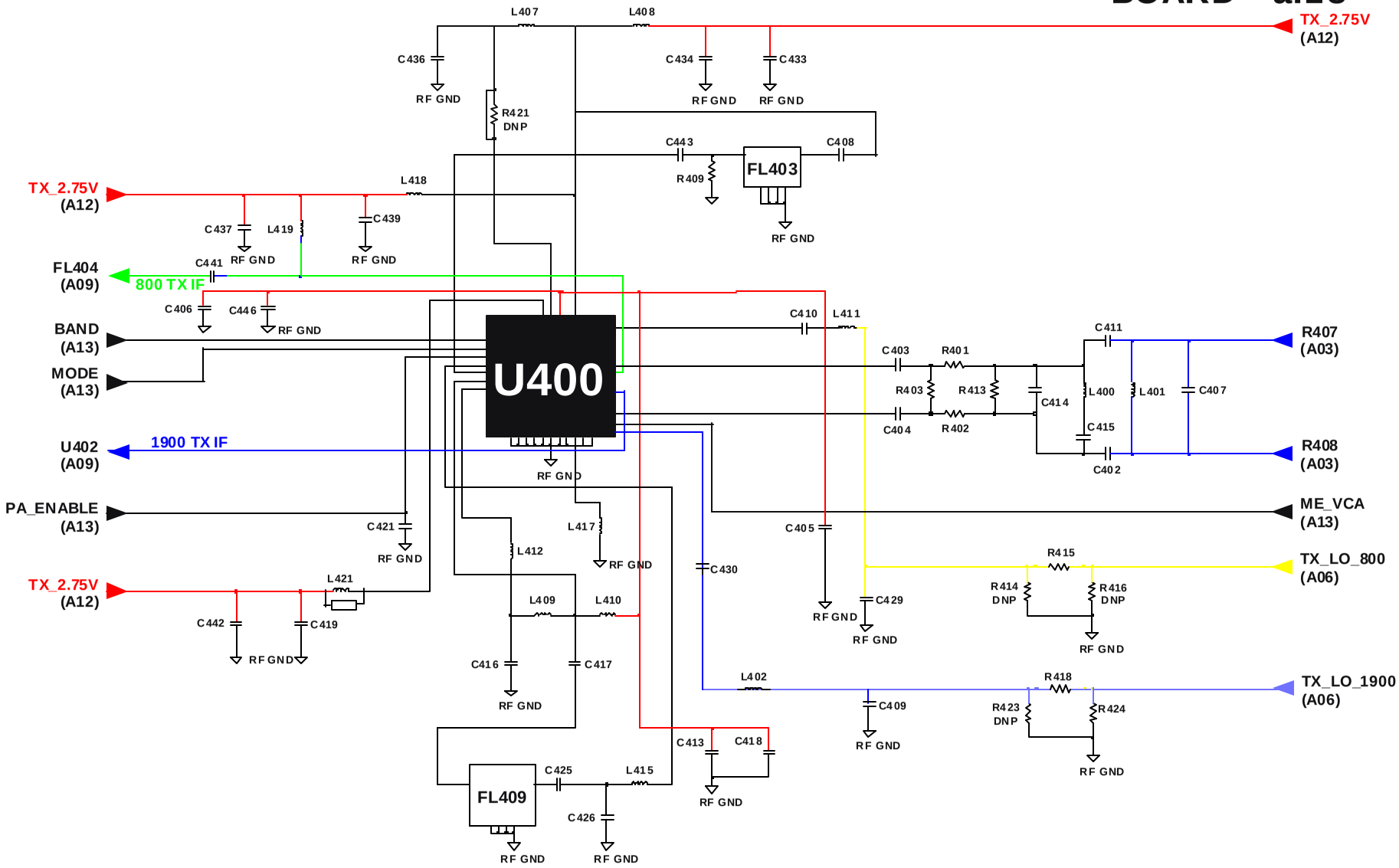

ME3:A08

V60i

1900 PA Circuit

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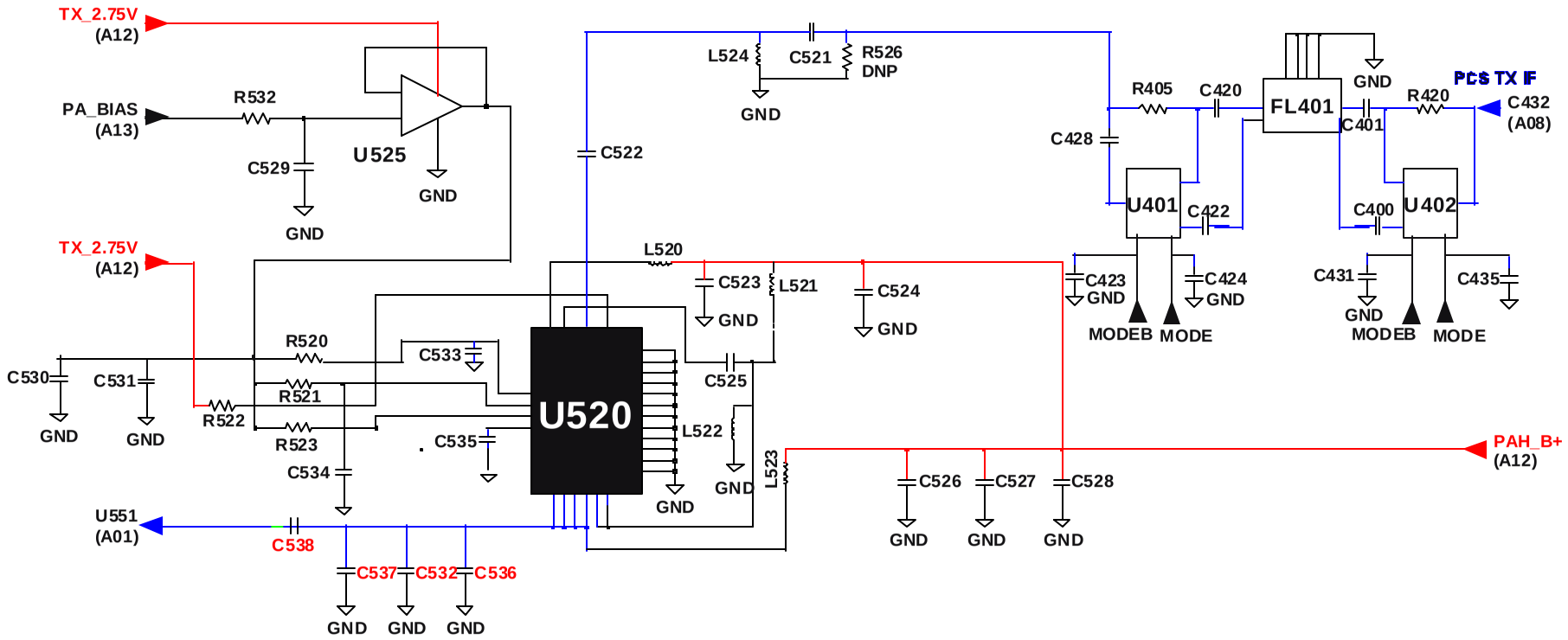

PA:A09

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800 PA Circuit

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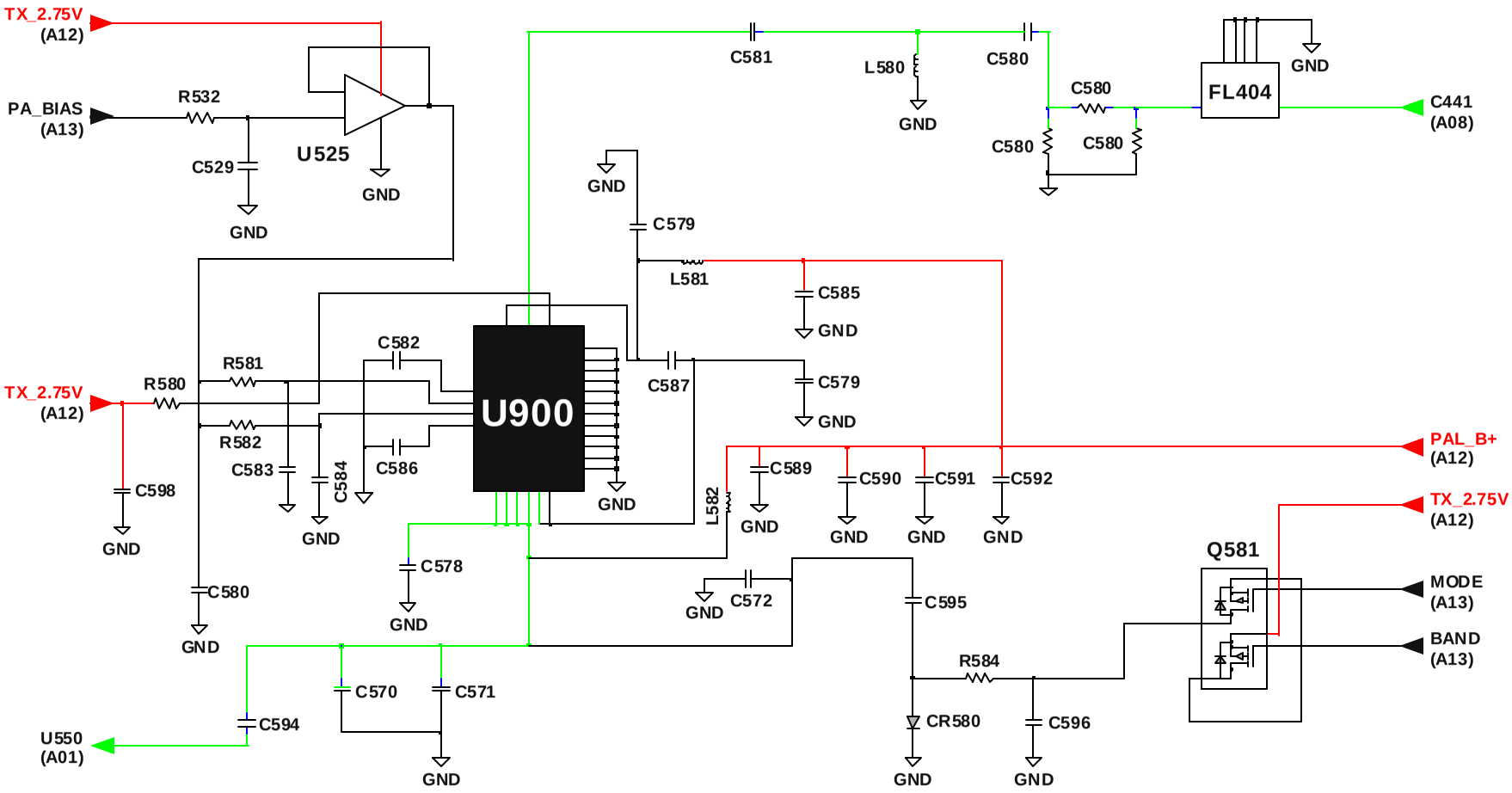

PA:A09

POWER DETECT & TEMP SENSE CIRCUIT

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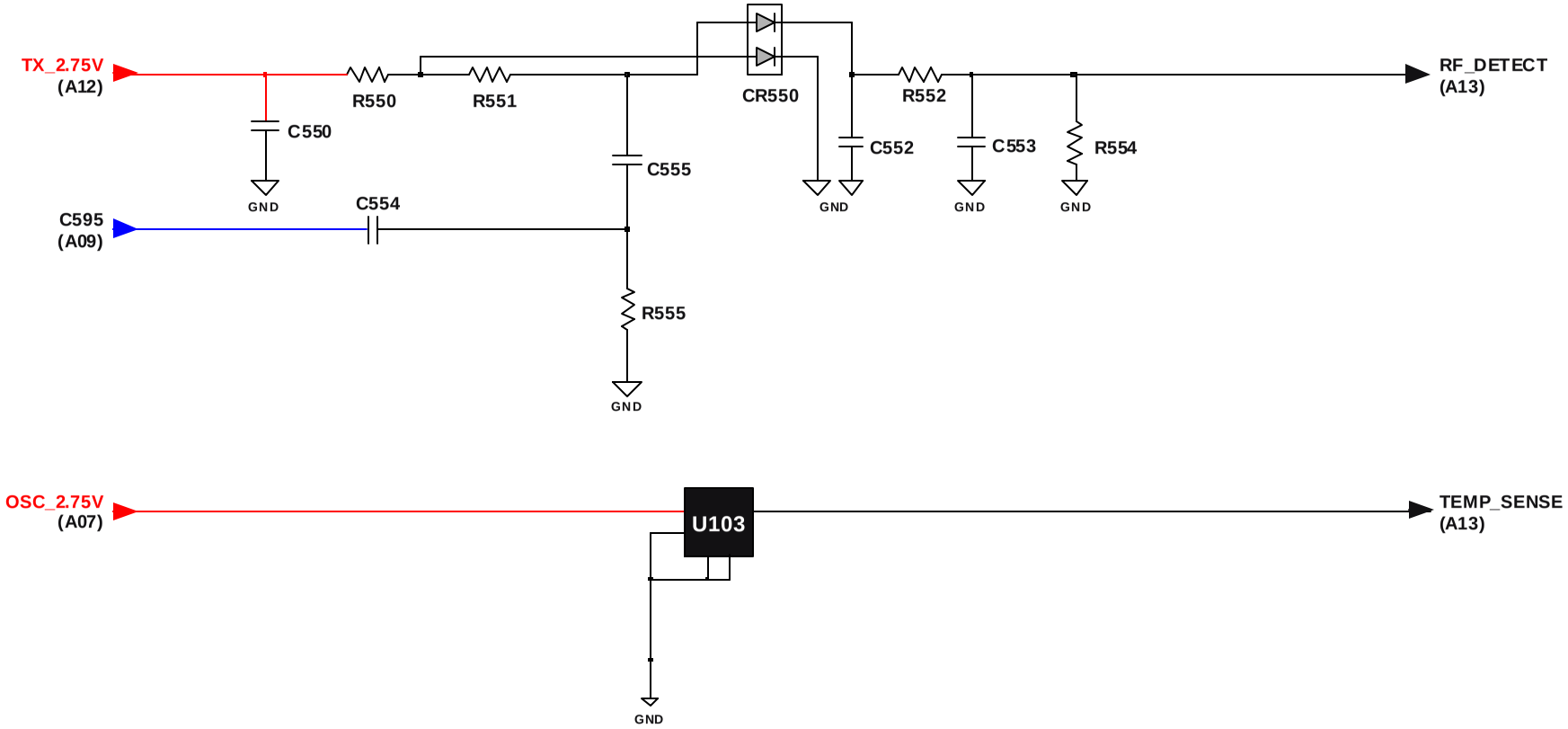

Power Detect & Temp Sense: A10

V60i

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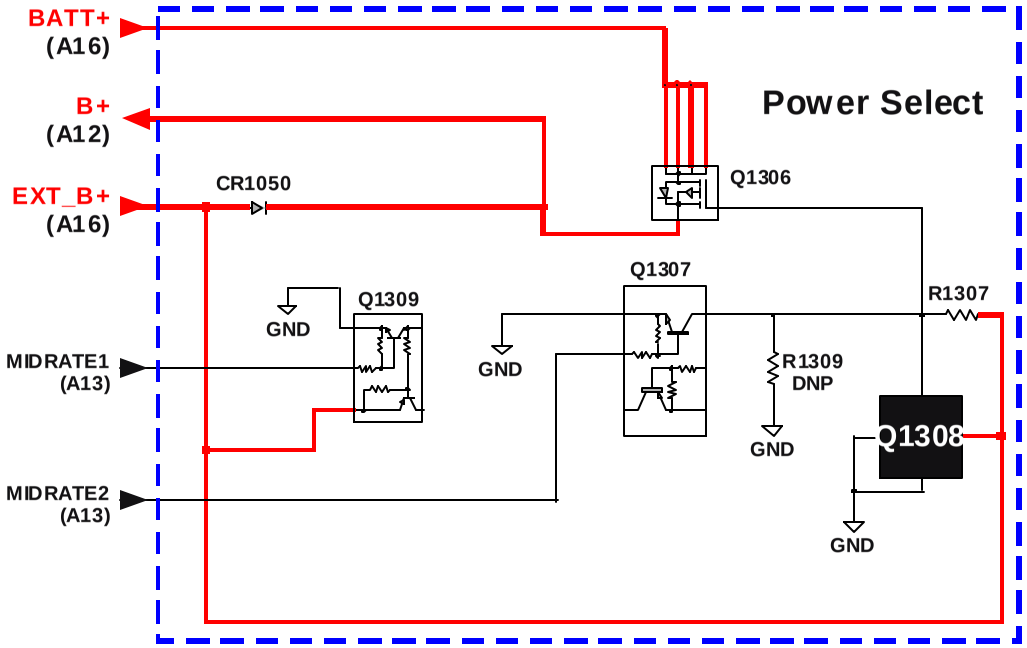

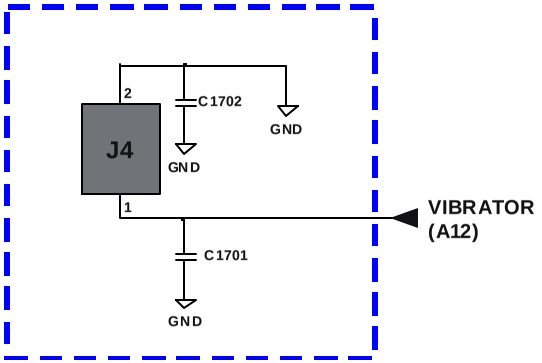

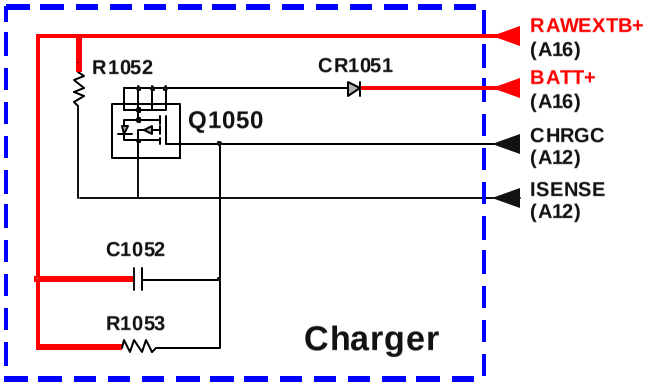

Power Select, Charger & Vibrator: A11

V60i

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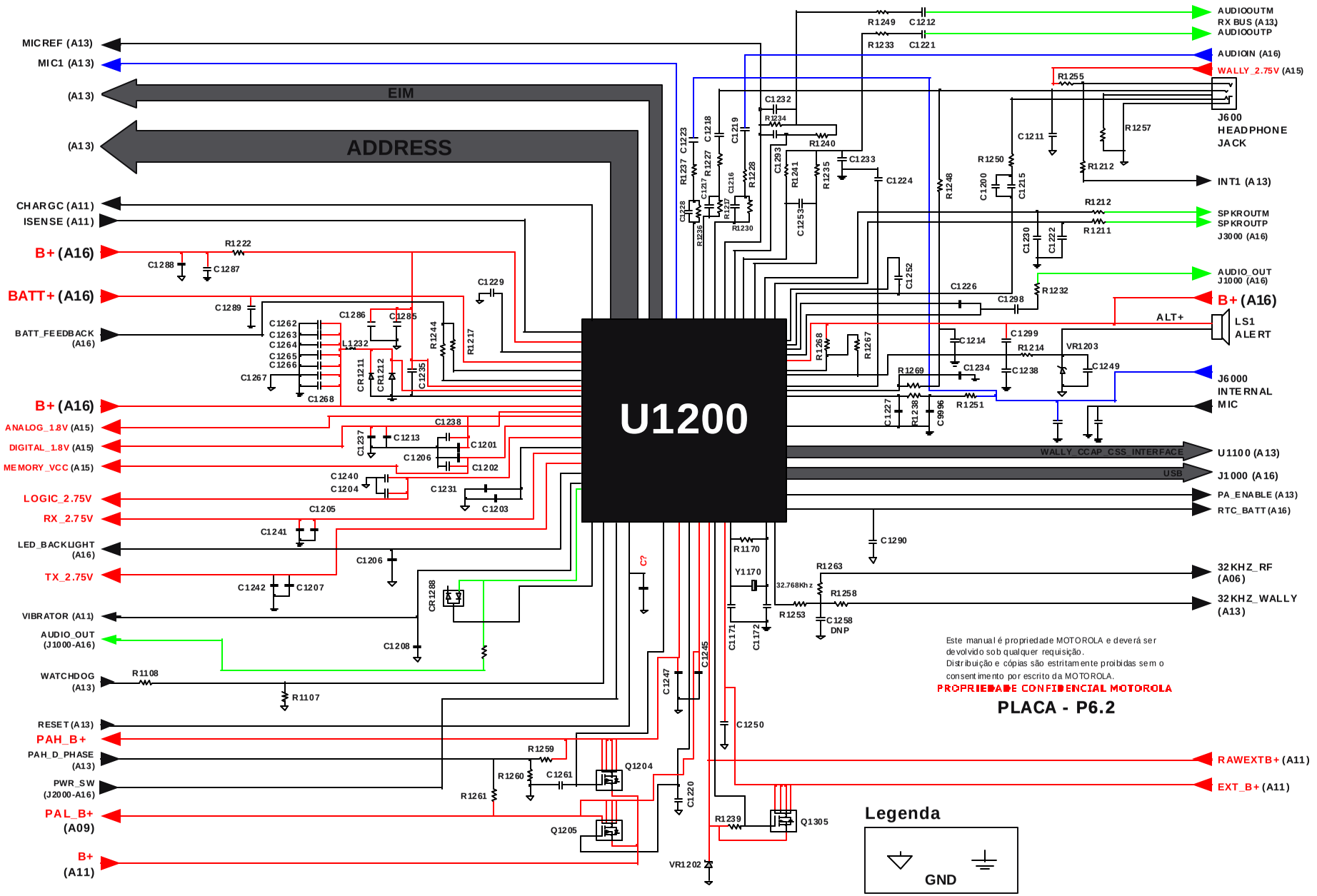

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PLACA - P6.2

Legenda

GND

CCAP:A12

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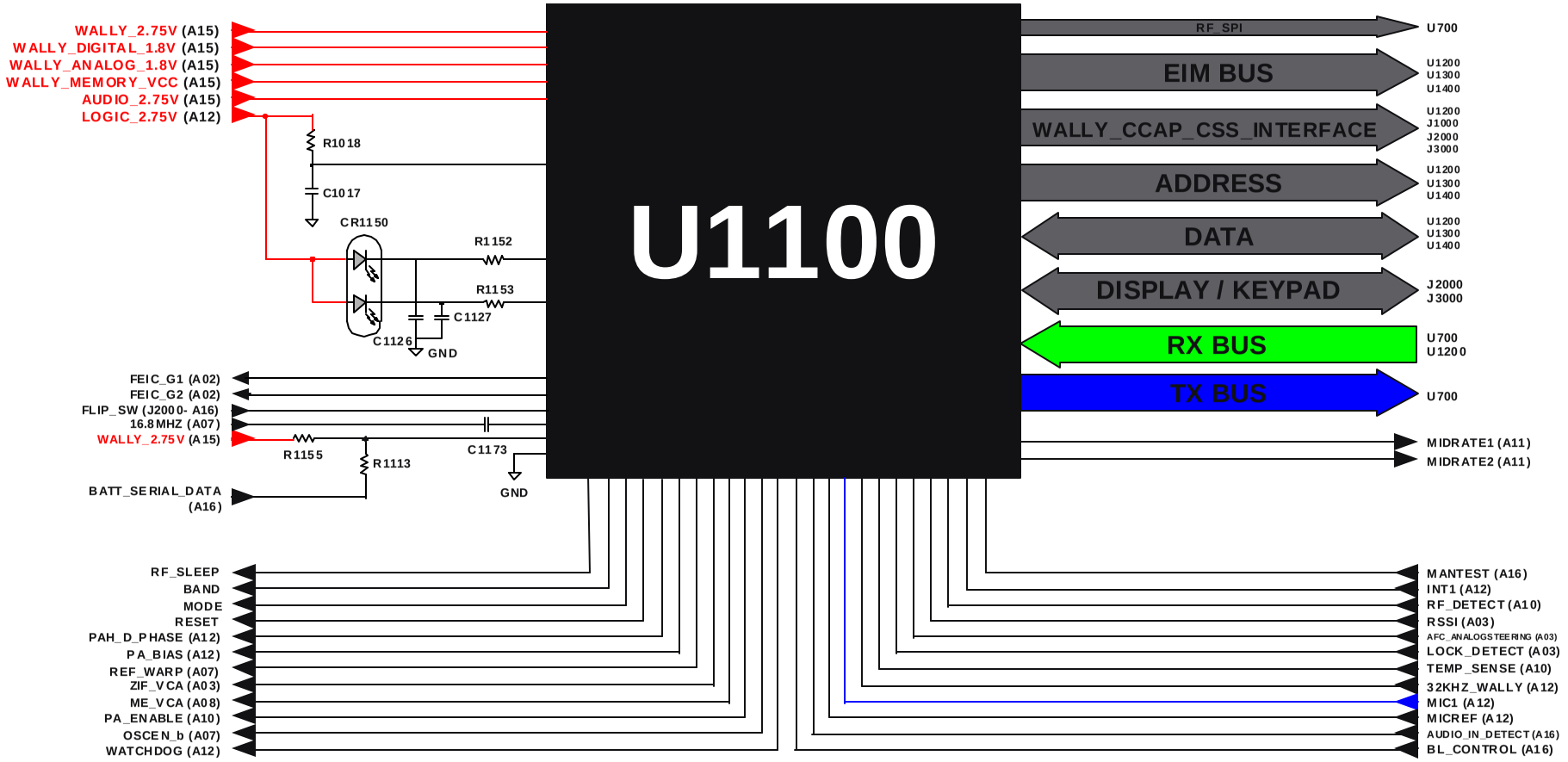

WALLY:A13

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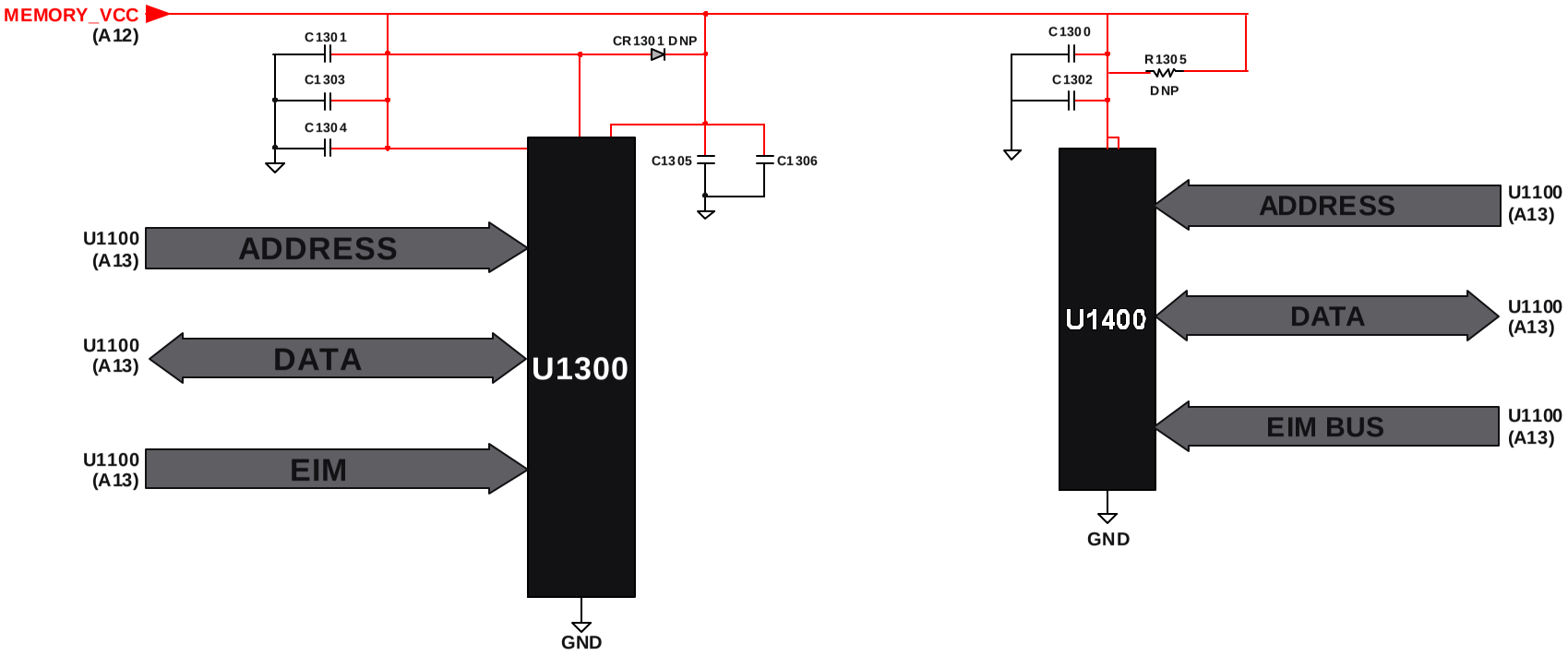

Memory:A14

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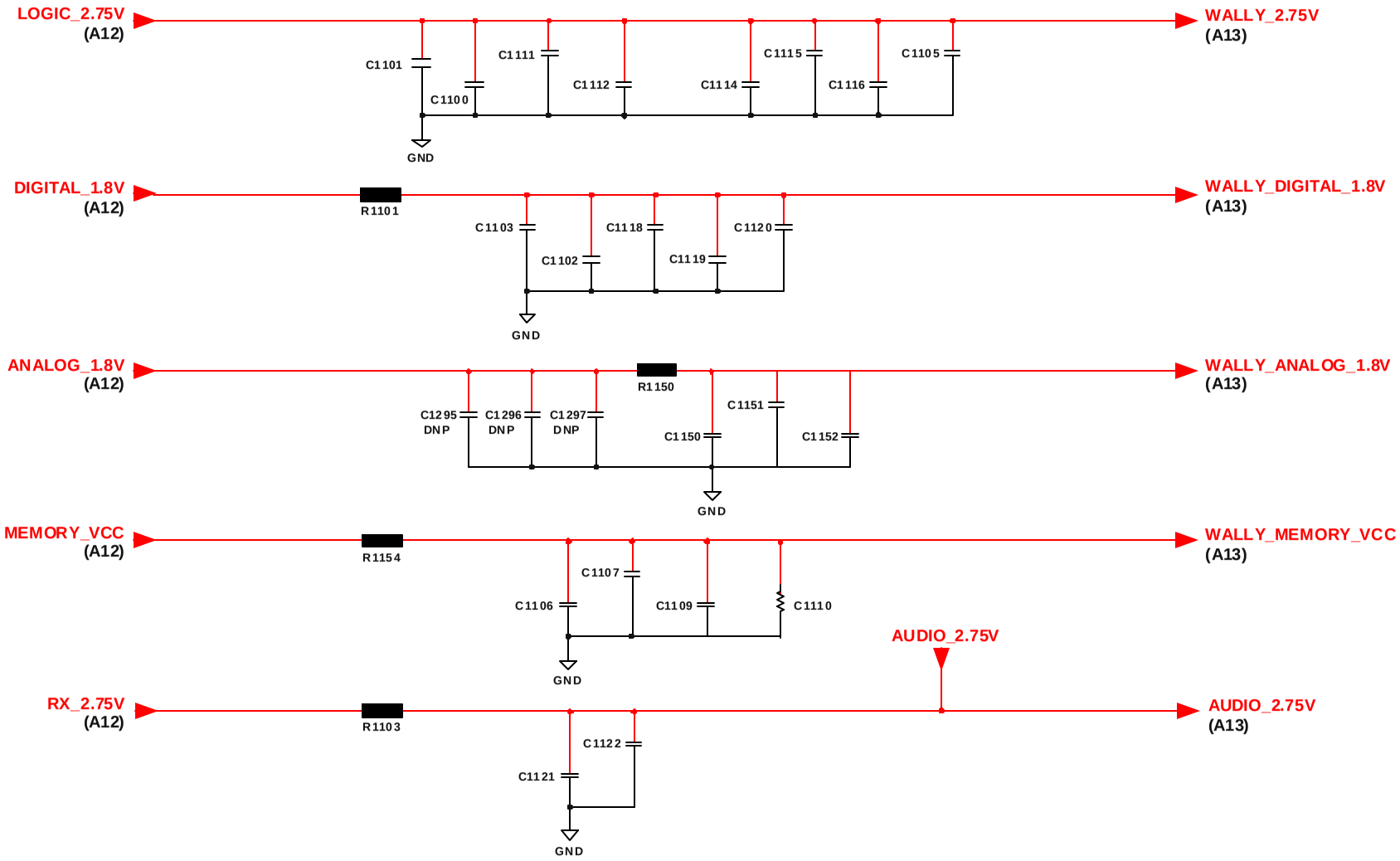

Power Distribuition:A15

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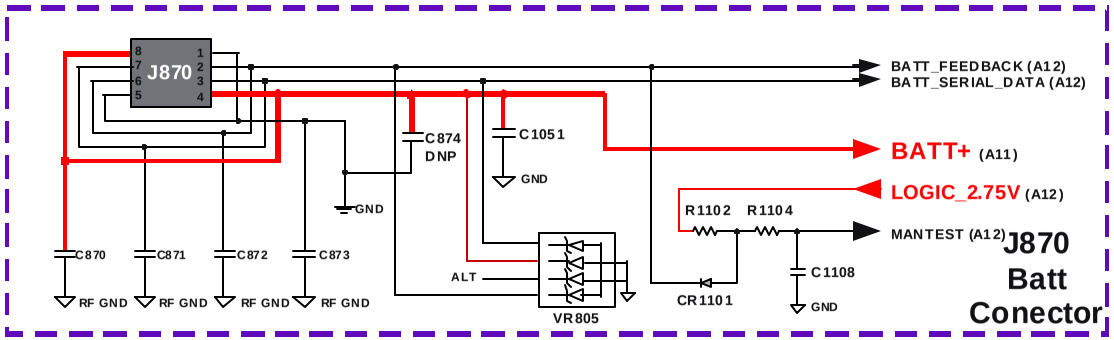

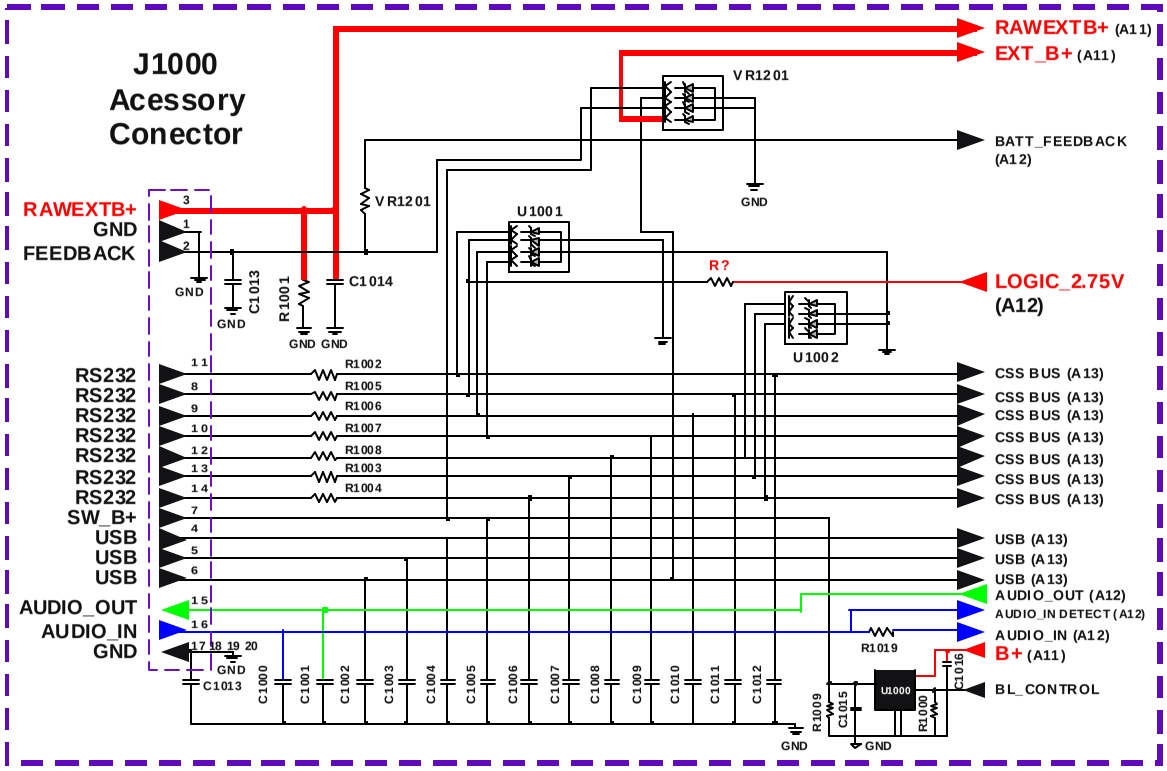

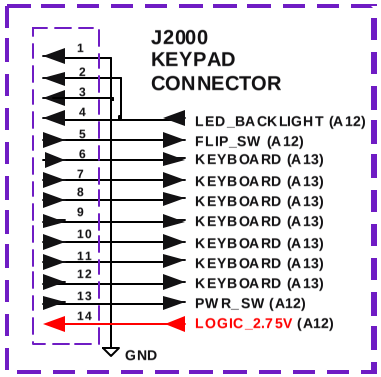

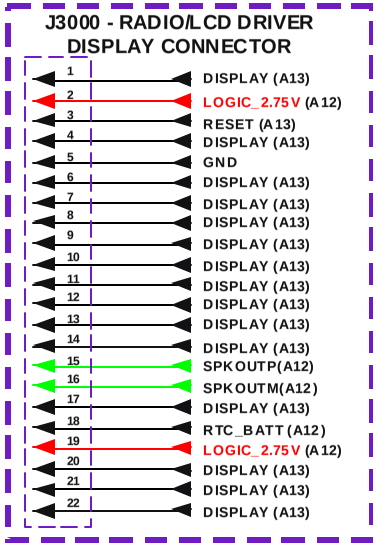

Connectors:A16

V60i RF BOARD LAYOUT

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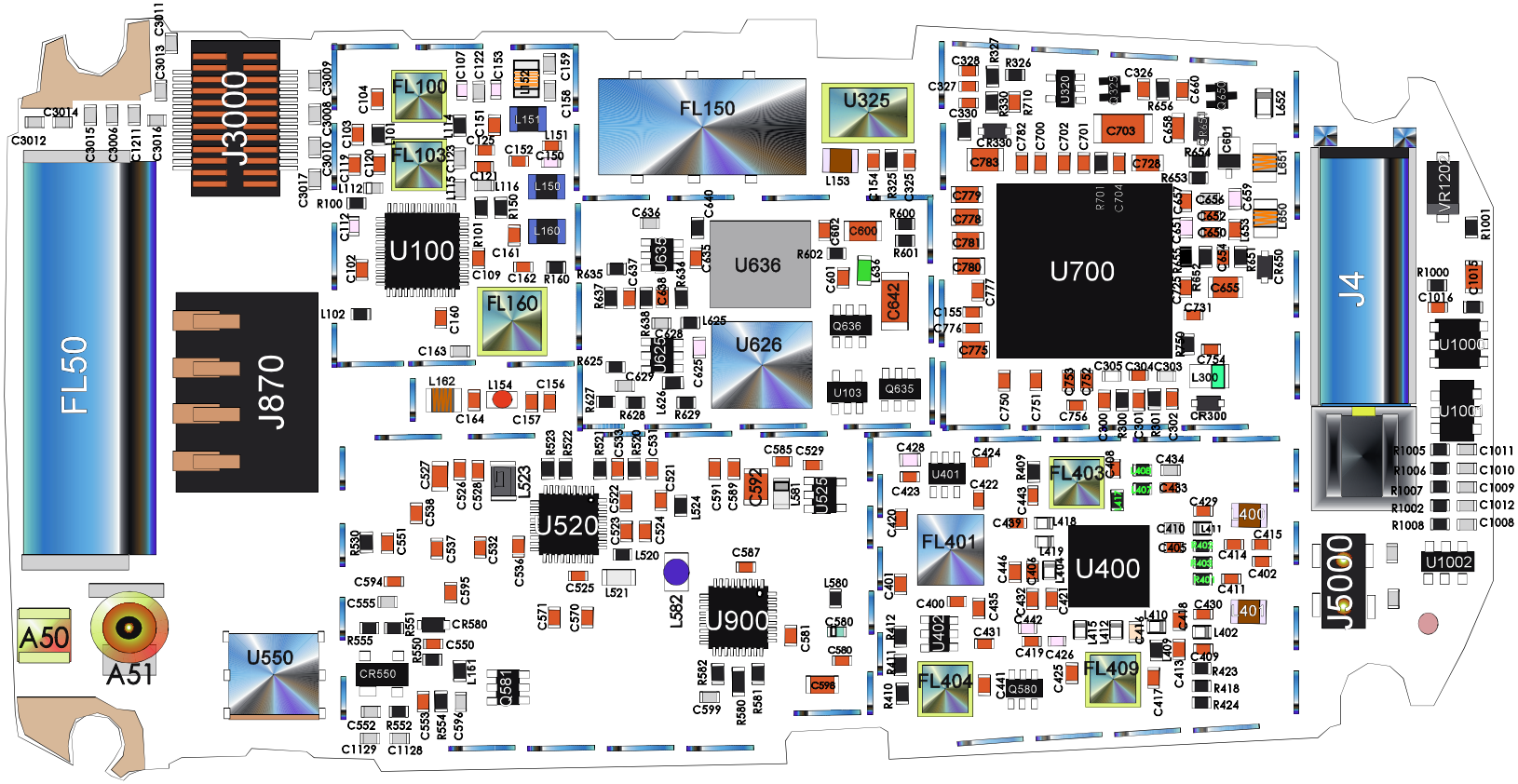

RF SIDE:A17

PHOENIX V60i A/L BOARD LAYOUT

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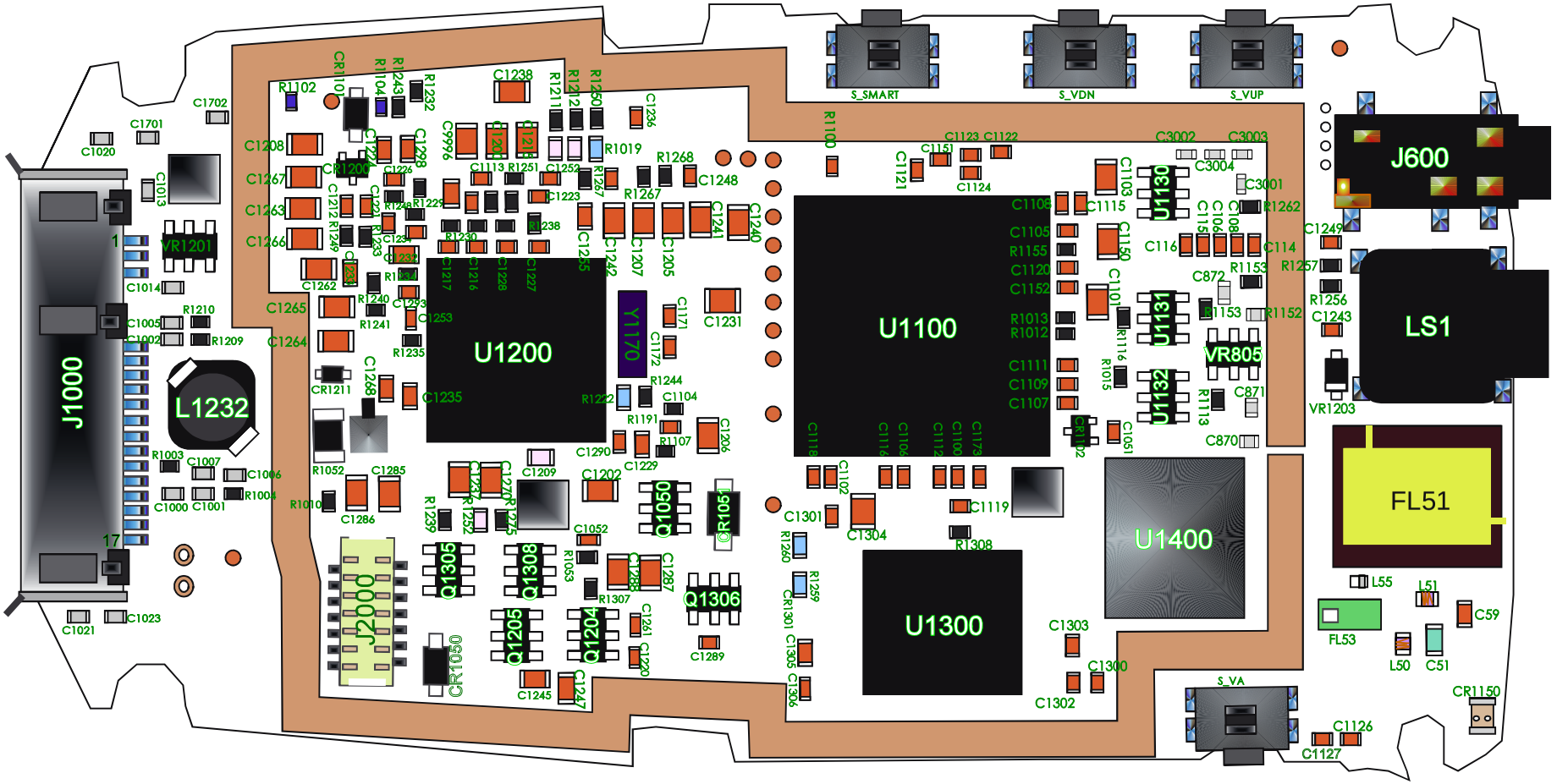

AUDIO LOGIC SIDE:A18