PIXELPLUS CO., LTD.

Preliminary
Data sheet

1/4 inch NTSC/PAL CMOS Image Sensor with 640 X 480 Pixel Array

PC7070K

Rev 0.0

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1/4 inch NTSC/PAL CMOS Image Sensor with 640 X 480 Pixel Array

▶ *Revision History*

Version	Date [D/M/Y]	Notes	Writer
0.0	29/10/2013	*(Preliminary)*	SangHyun Han

Caution : This datasheet can be changed without prior notice !! If you want to get up-to-date version, please send a mail to support@pixelplus.co.kr.

1/4 inch NTSC/PAL CMOS Image Sensor with 640 X 480 Pixel Array

▶ *Table of Contents*

1/4 inch NTSC/PAL CMOS Image Sensor with 640 X 480 Pixel Array

▶ Features

▷ 648 x 488 Effective pixel array with
RGB bayer color filters and micro-lens.
▷ Power supply :
HVDD/CVDD/AVDD=3.3V

▷ Input. Clock Frequency : 27MHz
▷ Output formats :
◆ Composite Output mode :
- CVBS (NTSC/PAL)
◆ Analog/Digital Concurrent Output mode :
- ITU-R. BT656 (720x240/288)
(interlaced, 60 fields/50fields @ 27MHz)
- CVBS (30 fps / 25 fps @ 27MHz)
▷ Image processing on chip : lens shading,
gamma / defect / color correction,
low pass filter, color interpolation, saturation,
edge enhancement, brightness, contrast,
auto black level , auto white balance,
auto exposure control
and back light compensation
▷ High Image Quality and Ultra low light
performance
▷ I2C master include
▷ GPO pads support
▷ Chip Address Selection PAD
▷ Horizontal / Vertical mirroring
▷ 50Hz, 60Hz flicker automatic cancellation
▷ Software Reset
▷ IR-LED control with CdS
▷ Crystal input support
▷ On chip regulator for DVDD
▷ CLCC/PLCC Package type supports

Parameter	Typical value
Pixel Size	5.60 um x 5.60 um
Effective Pixel Array	648 (H) x 488(V)
Effective Image Area	3.63 mm x 2.73 mm
Optical Format	1/4 inch
Input Clock frequency	27MHz
Frame Rate	NTSC : 60 field / sec PAL : 50field / sec
Dark Signal	TBD
Sensitivity	TBD
Power Supply	Analog : 3.3V HVDD : 3.3V CVDD : 3.3V
Power Consumption	TBD
	TBD
Operating Temp. (Fully Functional Temp)	TBD
Dynamic Range	TBD
SNR	TBD

[Table 1] Typical Parameters

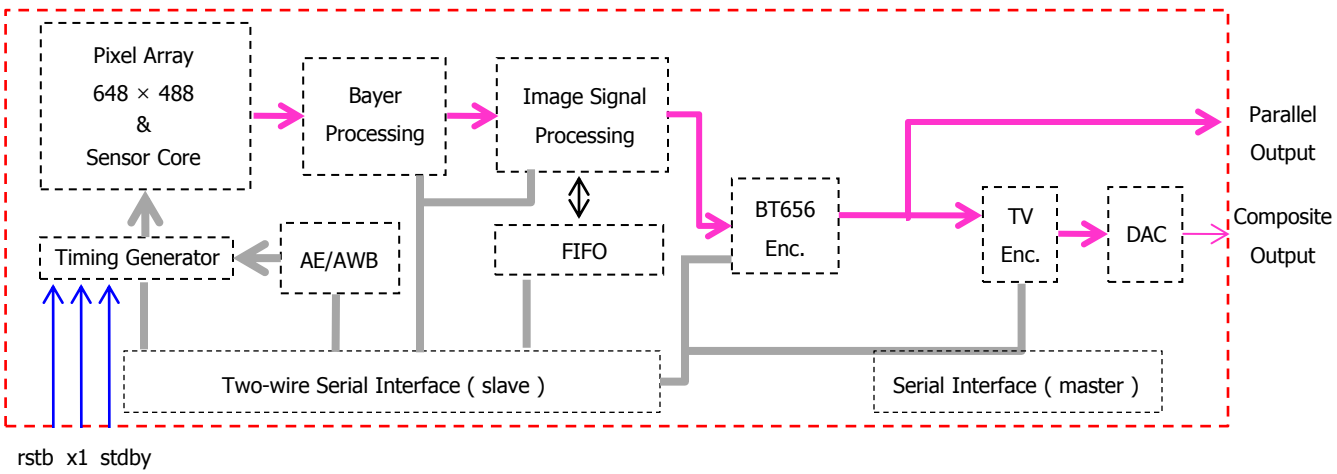
1/4 inch NTSC/PAL CMOS Image Sensor with 640 X 480 Pixel Array

▶ *Signal Environment*

PC7070K don't have tolerant Input pads. The input signal must be equal to HVDD for stable operation. If the power of input signal is higher than recommended , it may flow leakage current by shot circuit path in the input PADs.

▶ *Chip Architecture*

PC7070K has 648 x 488 effective pixel array and column/row driver circuits to read out the pixel data progressively. CDS circuit reduces noise signals generated from various sources mainly resulting from process variations. Pixel output is compared with the reset level of its own and only the difference signal is sampled, thus reducing fixed error signal level. Each of R, G, B pixel output can be multiplied by different gain factors to balance the color of images in various light conditions. The analog signals are converted to digital forms one line at a time and 1 line data are streamed out column by column. The Bayer RGB data are passed through a sequence of image signal processing blocks to finally produce YCbCr 4:2:2 output data. Image signal processing includes such operations as gamma correction, defect correction, low pass filter, color interpolation, edge enhancement, color correction, contrast stretch, color saturation, white balance, exposure control and back light compensation. Internal functions and output signal timing can be programmed simply by modifying the register files through 2-wire serial interface.



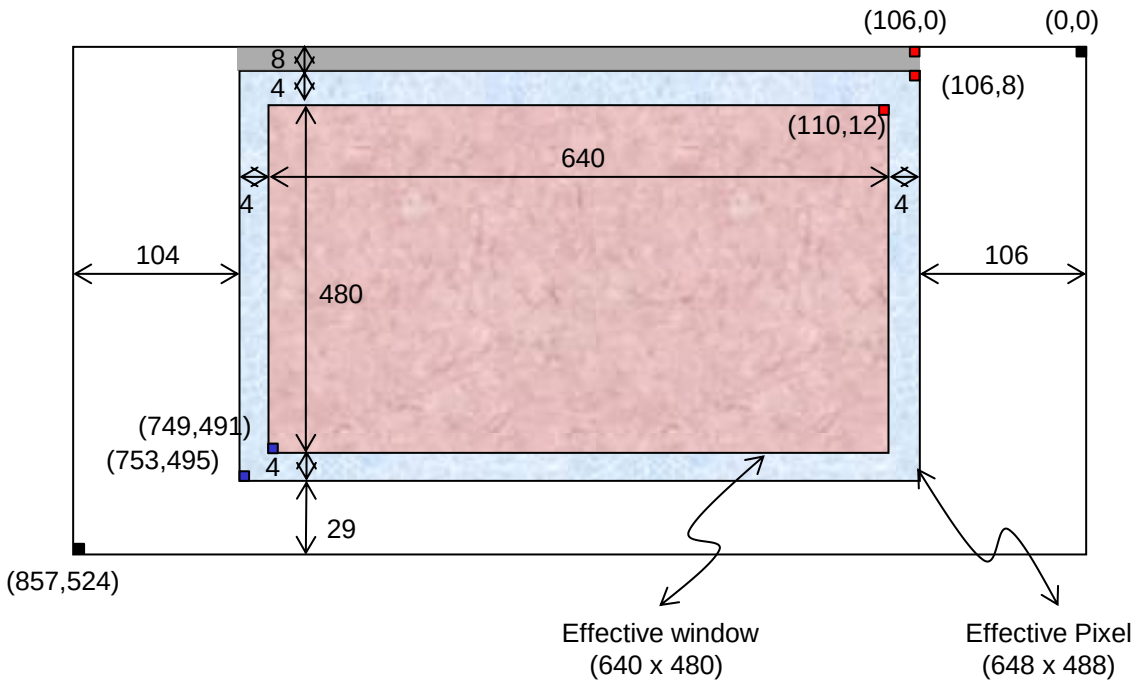
[Fig. 1] Block Diagram

1/4 inch NTSC/PAL CMOS Image Sensor with 640 X 480 Pixel Array

▶ *Frame Structure*

Origin *(0, 0)* of the frame is at the upper right corner. Size of the frame is determined by two registers : *framewidth(Reg.A-06h, A-07h)* and *frameheight(Reg.A-08h, A-09h).* One frame consists of *framewidth + 1* columns and *frameheight + 1* rows. *framewidth* and *frameheight* can be programmed to be larger than total array size. Effective window array of 640 x 480 pixels is positioned at *(110, 12).* Pixel scanning begins from *(0, 0)* and proceeds row by row downward, and for each line scan direction is from right to the left. Hsync signal indicates if the output is from a pixel that belongs to the window or not. There are two counters to indicate the present coordinate of frame scanning : Frame row counter and frame column counter. Counter values repeat the cycle of 0 to *frameheight* , and 0 to *framewidth* respectively. The counter values increase at the pace of pixel clock (pclk), which does not change as the frame size is altered. The pixel data rate is fixed and is independent of frame size.

PC7070K Frame Structure



[Fig. 2] Default Data Structure of Frame (Top View)

▶ Data and Synchronization Timing

1) Data Output Timing Diagram

[Fig. 3] shows the default data sequence of PC7070K. In [Fig. 3] VSYNC/HSYNC/PCLK polarity can have any combinations possible. Data can be latched at the rising or falling edge of PCLK. HSYNC can be set to be active high or active low. The sequence default YCbCr data is [Cb,Y, Cr, Y, …] for common even / odd rows.

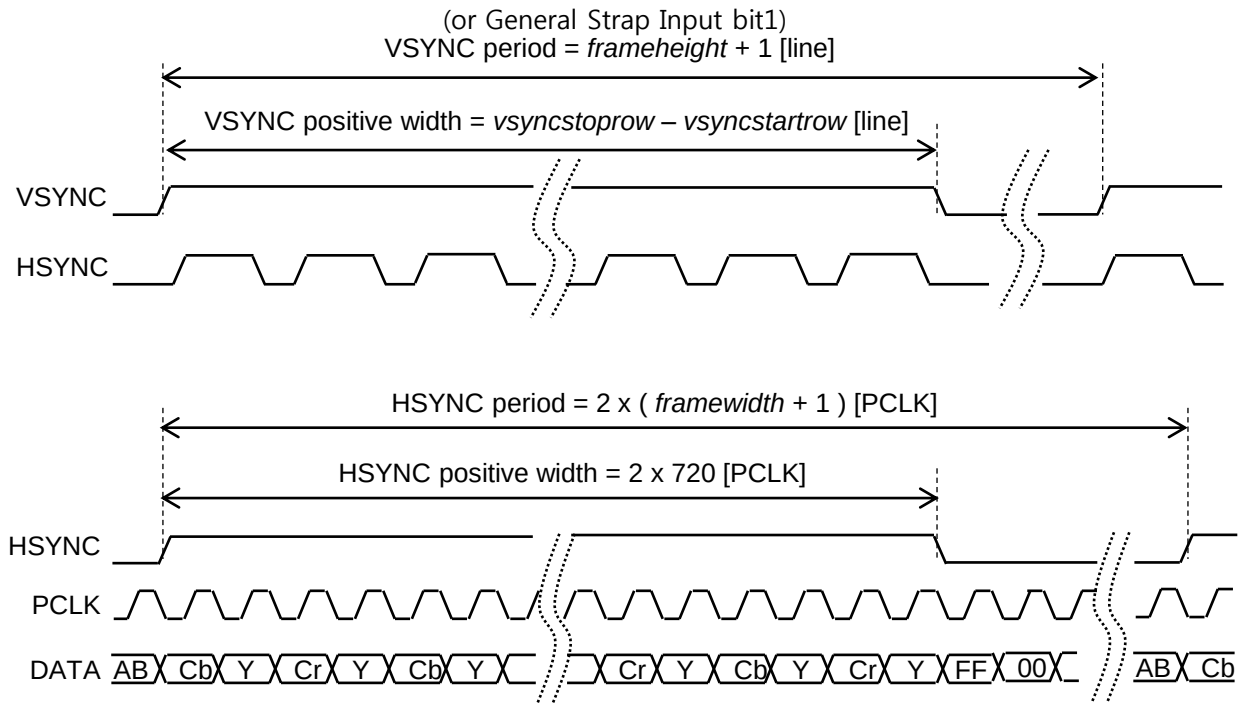
The positive width of VSYNC can be programmed by *vsyncstartrow* and *vsyncstoprow* (register value) and given by

VSYNC positive width = *vsyncstartrow* – *vsyncstoprow* [line]

The positive width of HSYNC is given by

HSYNC positive width = 2 x 720 [PCLK]

Data value can be selected in Invalid or blanking region.



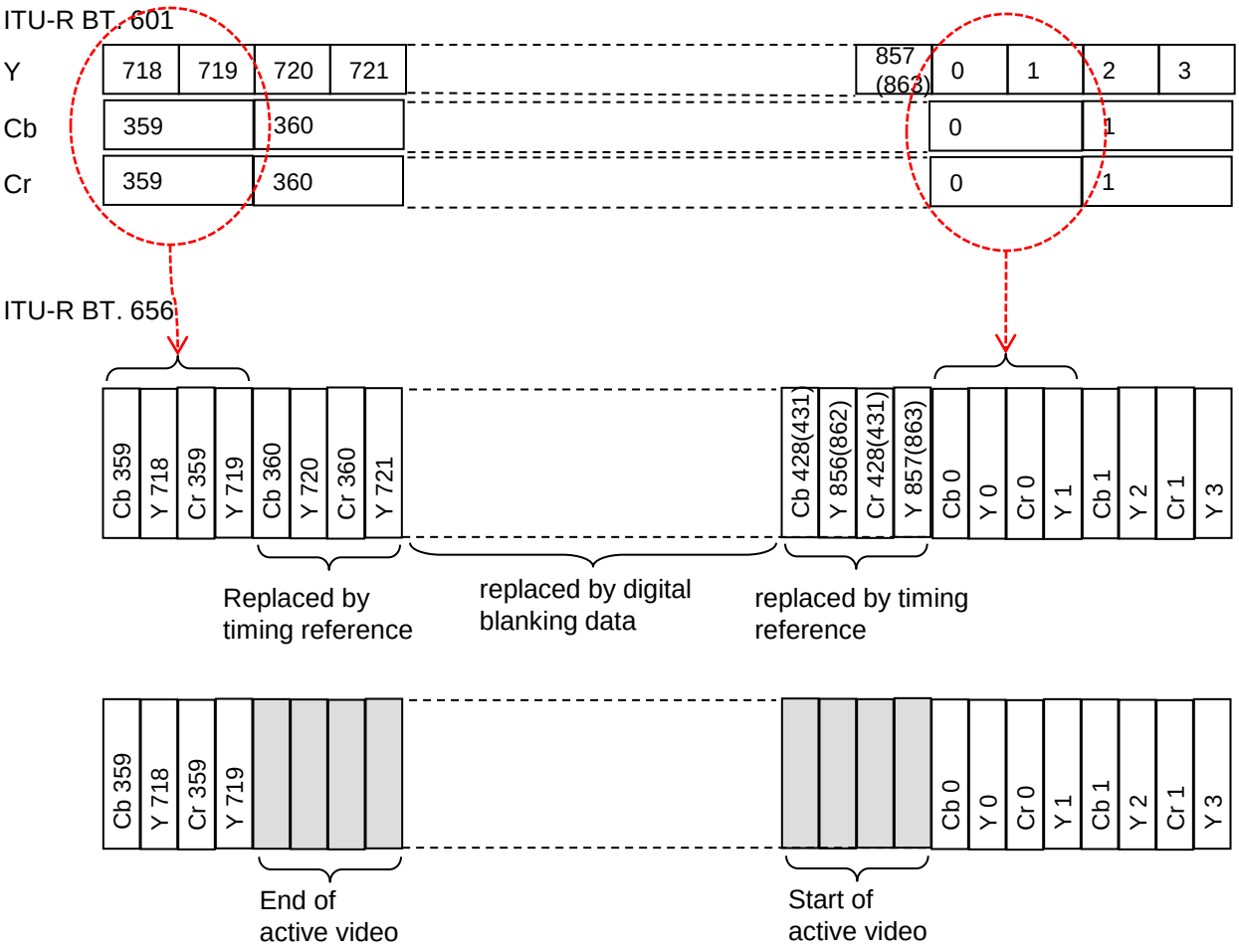
[Fig. 3] Timing Diagram for VSYNC, HSYNC, PCLK and Data

▶ Data and Synchronization Timing

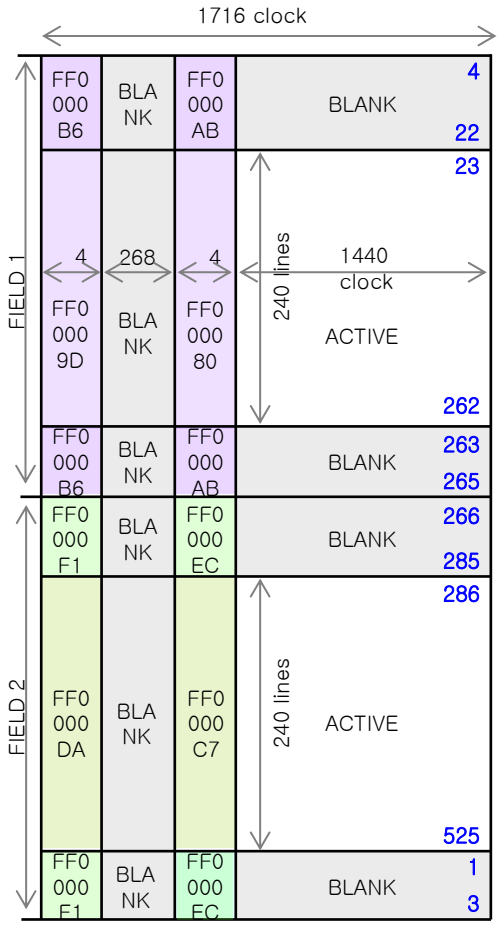
2) ITU-R BT656 (CCIR656)

[Fig. 4] shows ITU-R BT601 and ITU-R BT656 timing diagram. Sampling clocks of ITU-R BT601 and ITU-R BT656 are 13.5MHz and 27MHz respectively. ITU-R BT656 format is generated from ITU-R BT601 format data by serialization and timing reference. Timing reference indicates Start or End of video. It includes field, vsync and hsync information.

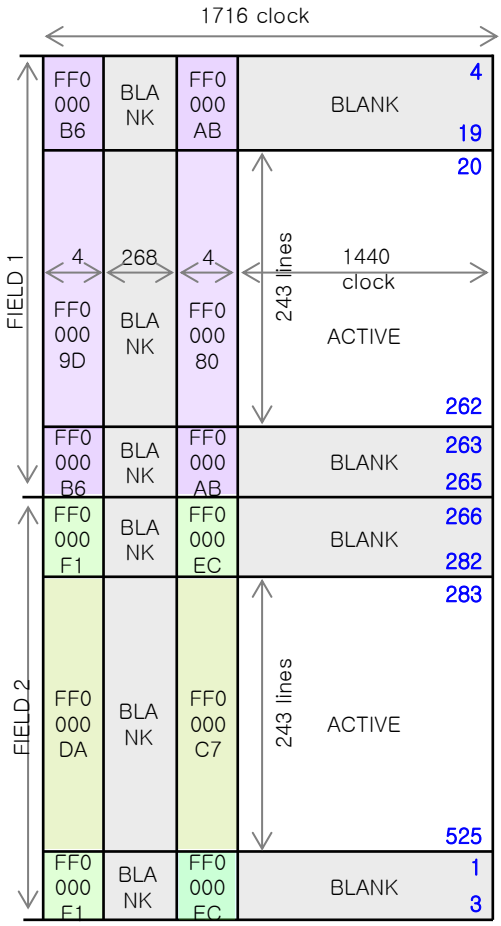
PC7070K provides two kinds of active video sizes with BT656 format such as 720x480i and 720x576i ('i' stands for interlaced scan). The horizontal size is stretched to 720 pixels. 720x480i size BT656 supports for 525-line video, and 720x576i size BT656 for 625-line video. Horizontal timing of 720x480i and 720x576i size BT656 is shown in [Fig. 4] and vertical Timing diagram is shown in [Fig. 5]



[Fig. 4] Timing Diagram of ITU-R BT601 and ITU-R BT656

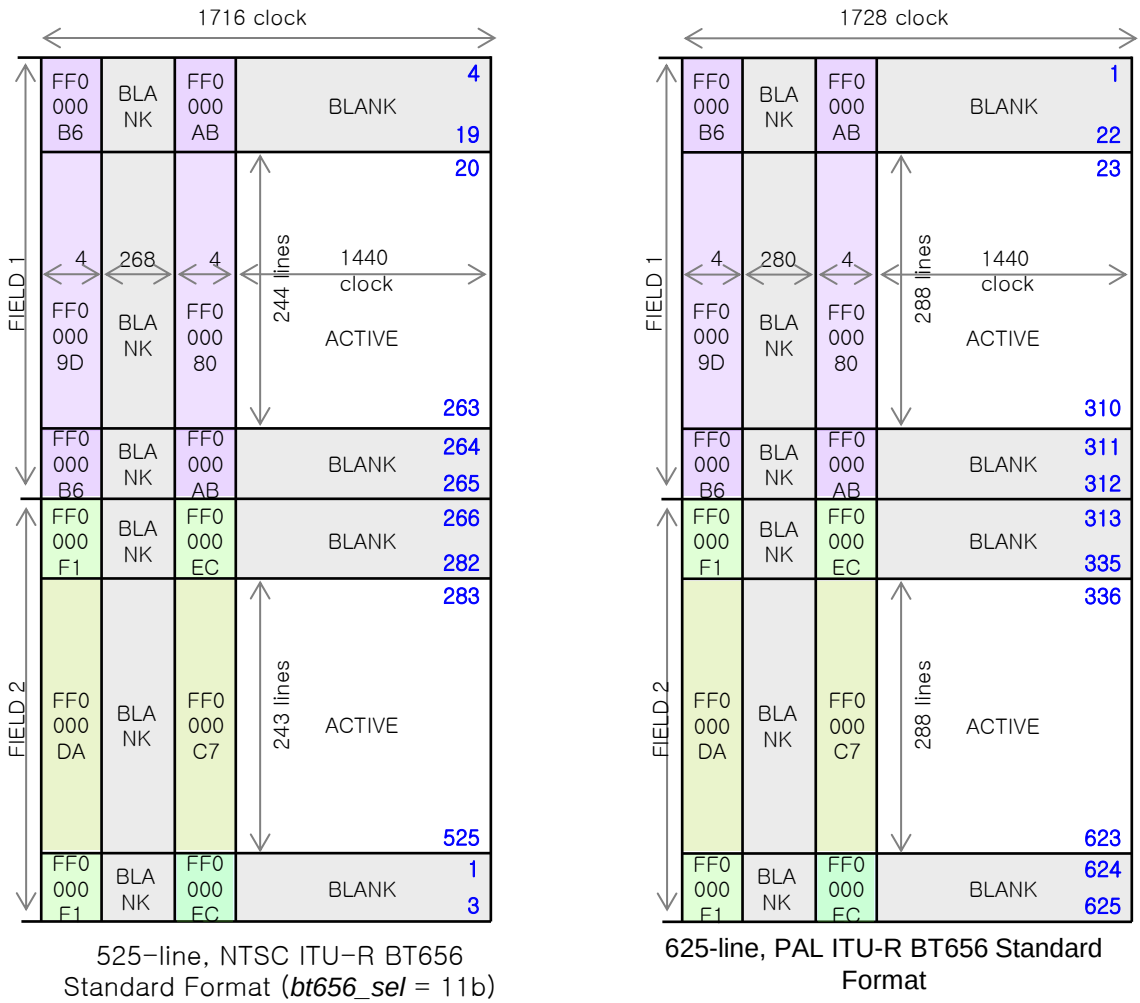


525-line, NTSC ITU-R BT656 Standard like Format (*bt656_sel* = 00b)



525-line, NTSC ITU-R BT656 Standard like Format (*bt656_sel* = 10b)

[Fig. 5] Vertical Timing Diagram of ITU-R BT656 (continue)



[Fig. 5] Vertical Timing Diagram of ITU-R BT656

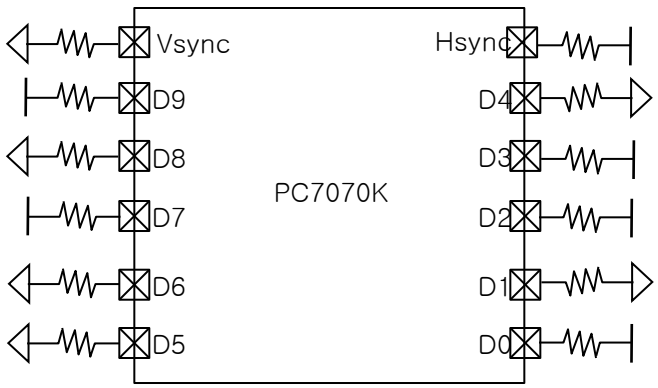
• The numbers on the image indicate Line number.

• For 525-line format, active lines are 240, 243 or 244 per a field. For 625-line format, active lines are 288 per a field.

• Vertical Timing is slightly different to Typical BT.656 for 525-line format. In active data regions above [Fig. 5] they have only active pixel data not any fixed data (eg. black data).

▶ *Wire-strapping*

Wire-strapping is a function of chip mode selection. Chip mode is automatically selected according to D9~D0 pads wired with pull-up or pull-down. [Fig. 6] shows an example of Wire-strapping configuration and [Table 2] shows chip mode selection by wire-strapping.



[Fig.6] Example of Wire-strapping

		vsync	hsync	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TV_MODE	(M)NTSC	-	-	-	-	-	-	-	L	L	L	-	-
	NTSC-J	-	-	-	-	-	-	-	L	L	H	-	-
	(M)PAL	-	-	-	-	-	-	-	L	H	L	-	-
	(Nc)PAL	-	-	-	-	-	-	-	L	H	H	-	-
	(B,D,G,H,I) PAL	-	-	-	-	-	-	-	H	L	L	-	-
	(N)PAL	-	-	-	-	-	-	-	H	L	H	-	-
	NTSC-4.43	-	-	-	-	-	-	-	H	H	L	-	-
FLICKER	No Flicker cancel	-	-	-	-	-	L	L	-	-	-	-	-
	Manual-A	-	-	-	-	-	L	H	-	-	-	-	-
	Manual-B	-	-	-	-	-	H	L	-	-	-	-	-
	Auto Flicker cancel	-	-	-	-	-	H	H	-	-	-	-	-
MIRROR	NO MIRROR	-	-									H	L
	MIRROR-V	-	-	-	-	-	-	-	-	-	-	L	L
	MIRROR-H	-	-	-	-	-	-	-	-	-	-	H	H
	MIRROR-VH	-	-	-	-	-	-	-	-	-	-	L	H
BLC(or (general[0])	ON	-	-	-	-	H	-	-	-	-	-	-	-
	OFF	-	-	-	-	L	-	-	-	-	-	-	-
Indoor/ Outdoor (or general[1])	Indoor mode	-	-	-	H	-	-	-	-	-	-	-	-
	Outdoor mode	-	-	-	L	-	-	-	-	-	-	-	-

[Table 2] Wire-strapping (continue)

		vsync	hsync	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Parking Guide Line	Enable	-	-	H	-	-	-	-	-	-	-	-	-
	Disable	-	-	L	-	-	-	-	-	-	-	-	-
MASTER MODE	ON	H	-	-	-	-	-	-	-	-	-	-	-
	OFF	L	-	-	-	-	-	-	-	-	-	-	-
General[2]	'1'	-	H	-	-	-	-	-	-	-	-	-	-
	'0'	-	L	-	-	-	-	-	-	-	-	-	-

[Table 2] Wire-strapping

[Table 3] shows TV_mode wire-strapping registers. These registers are changed by D4~D2.

Register name	"000b" (M)NTSC	"001b" NTSC-J	"010b" (M)PAL	"011b" (Nc)PAL	"100b" (OTHER) PALs	"101b" (N)PAL	"110b" NTSC-4.43
pad_control7	01	01	01	01	01	01	01
chip_mode	00	00	00	01	01	01	00
framewidth_h	03	03	03	04	04	04	03
framewidth_l	59	59	59	0D	0D	0D	59
fd_a_step_h	03	03	03	04	04	04	03
fd_a_step_l	E8	E8	E8	BD	BD	BD	E8
fd_b_step_l	40	40	40	F0	F0	F0	40
fd_period_a_h	01	01	01	00	00	00	01
fd_period_a_m	03	03	03	D8	D8	D8	03
fd_period_a_l	80	80	80	F8	F8	F8	80
fd_period_b_m	3B	3B	3B	01	01	01	3B
fd_period_b_l	0D	0D	0D	00	00	00	0D
fd_period_c_h	06	06	06	05	05	05	06
fd_period_c_m	27	27	27	15	15	15	27
fd_fheight_a_l	0C	0C	0C	07	07	07	0C
fd_fheight_b_l	0C	0C	0C	07	07	07	0C
expfrmH_l	07	07	07	02	02	02	07
midfrmheight_l	07	07	07	02	02	02	07
maxfrmheight_l	07	07	07	02	02	02	07
vsyncstoprow_f0_l	06	06	06	36	36	36	06
vsyncstartrow_f1_l	1E	1E	1E	50	50	50	1E
vsyncstoprow_f1_l	0D	0D	0D	6F	6F	6F	0D
osd_efld_s_h	00	00	00	00	00	00	00
osd_efld_s_l	01	01	01	01	01	01	01
osd_ofld_s_h	01	01	01	01	01	01	01
osd_ofld_s_l	0A	0A	0A	39	39	39	0A
enc_mode	00	00	03	02	01	01	00
enc_blankL	F0	F0	F0	FC	FC	F0	F0
enc_pedestal	2A	00	2A	00	00	2A	2A
enc_burst	80	82	8C	8A	9C	9A	82
enc_Ygain	82	8D	82	89	89	82	82
enc_Ugain	6F	78	6F	75	75	6F	6F
enc_Vgain	9C	A9	9C	A6	A6	9C	9C
enc_Crange_L	48	62	48	5B	5B	48	48
enc_chroma_max_L	CD	DF	CD	D7	D7	CD	CD
enc_chroma_min_L	6D	35	6D	45	45	6D	6D
enc_scfreq	00	00	03	02	01	01	01
hsync_p_toffset	12	12	12	00	00	06	12
burst_duration	00	00	89	89	00	00	8D
l_blank_start	0C	0C	0D	12	15	10	0C
l_blank_stop	02	02	03	0B	0B	00	02
sync_rising	04	04	04	08	08	07	04
burst_toffset	88	88	08	8A	96	96	88
encdat_rising	04	04	04	07	08	07	04
setup_w	07	00	07	00	00	07	07

[Table 3] TV Mode Registers

[Table 4~7] show registers and setting values related with Flicker mode, Mirror mode, BLC mode and Indoor/Outdoor mode.

	"00b"	"01b"	"10b"	"11b"
Register name	Normal(off)	manual A	manual B	auto_fd
flicker_control_1	00	08	04	40

[Table 4] Flicker Mode Register

	"00b"	"01b"	"10b"	"11b"
Register name	V mirror	HV mirror	No mirror	H mirror
mirror	02	03	00	01

[Table 5] Mirror Mode Register

	vsync="0b"	vsync="1b"	vsync="1b"
Register name		BLC off ("0b")	BLC on ("1b")
ae_weight1	08	08	08
ae_weight2	08	08	08
ae_weight3	08	08	08
ae_weight4	08	08	08
ae_weightc	08	08	38
max_yt1	A0	A0	A0
max_yt2	80	80	80
min_yt1	78	78	78
min_yt2	78	78	78

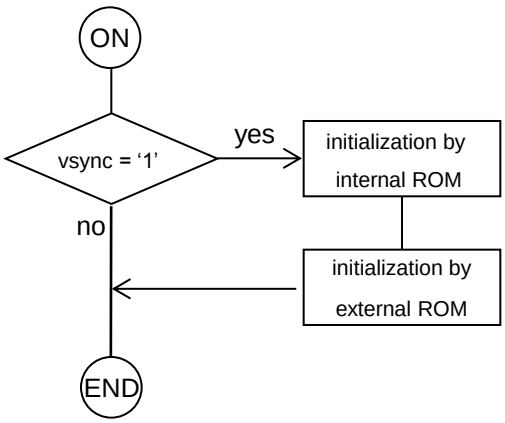
[Table 6] BLC Mode Register

	vsync="0b"	vsync="1b"	vsync="1b"
Register name		Outdoor ("0b")	Indoor ("1b")
awb_rgain_min	00	64	00
awb_rgain_max	00	90	FF
awb_bgain_min	FF	54	00
awb_bgain_max	FF	68	FF

[Table 7] Indoor/Outdoor Mode Register

Caution : If sensor is operated by not master mode (vsync = "0b") BLC, Indoor/Outdoor strap is can't be operated. (adaptive fixed value)

[Table 8] show registers and setting values related with master mode.



[Fig. 7] shows initialization process of registers. When vsync is high, register default values are initialized by internal ROM and external ROM.

▶ If you want to see more processes, see [Fig. 10].

[Fig. 7] Initialization Process of Registers

Registers	vsync = 0b master mode off	vsync = 1b master mode on

Registers	vsync = 0b master mode off	vsync = 1b master mode on

[Table 8] Internal ROM Registers Setting (continue)

Registers	vsync = 0b master mode off	vsync = 1b master mode on

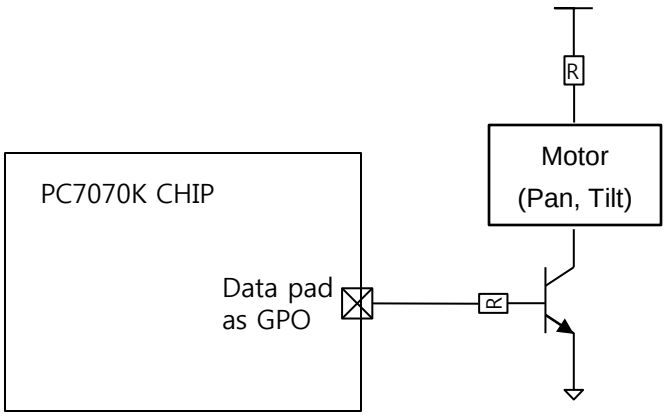
Registers	vsync = 0b master mode off	vsync = 1b master mode on

[Table 8] Internal ROM Registers Setting

▶ Data Pads as GPO

Data pads(D9~D2) can be used as GPO(General Purpose Output) when user doesn't use digital output. If *reg_pad_control3*[0] is set to '1b', user can control data pads outputs manually by setting *reg_pad_control9*.

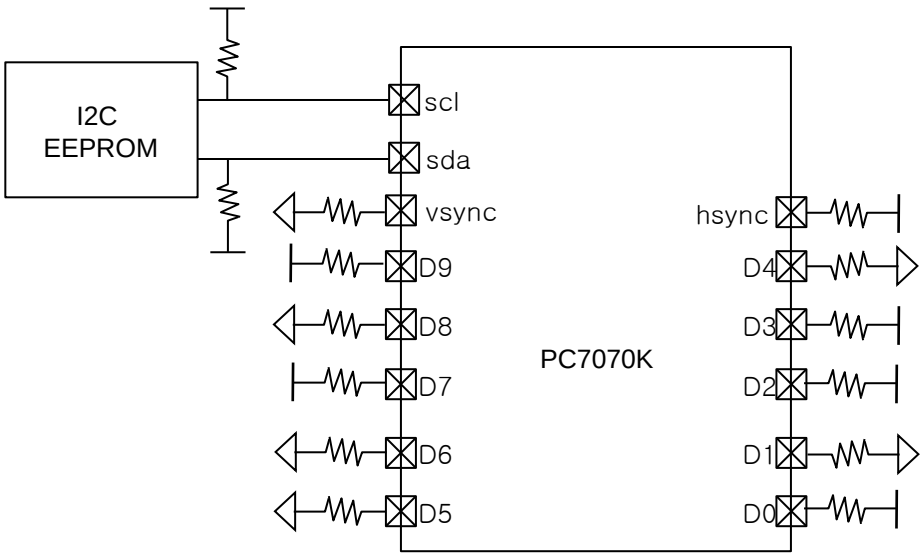
[Fig. 8] shows an example of using GPO pad. User can control a motor to pan or tilt the sensor module by controlling GPO pad data.



[Fig. 8] Example of Using GPO Pad

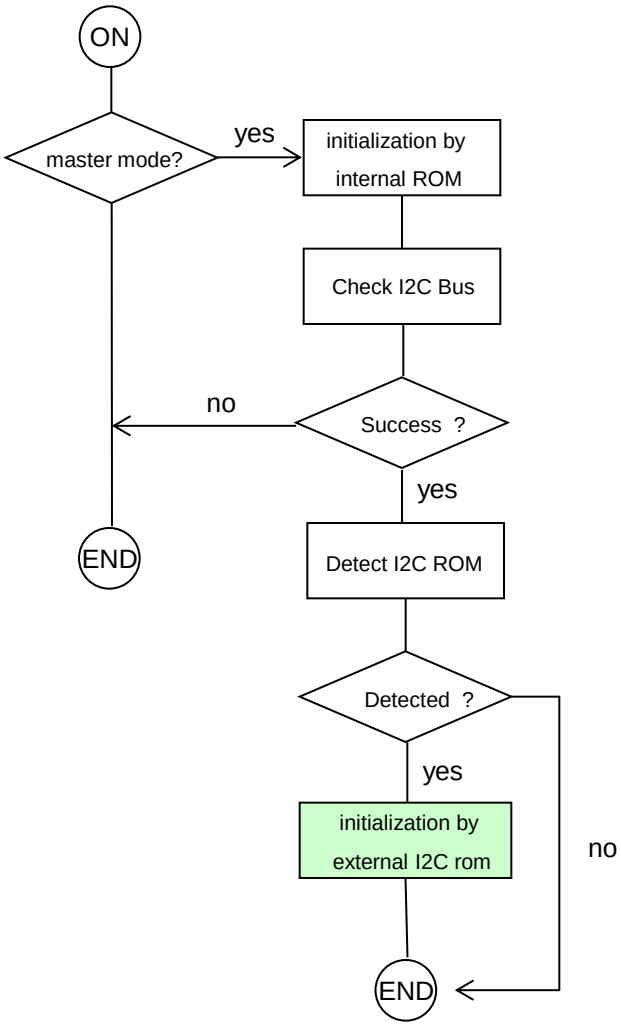
▶ Registers Initializing

PC7070K supports user tuning registers can be set by I2C EEPROM initially. [Fig. 9] shows how to connect PC7070K with external ROM(I2C EEPROM). After reset, PC7070K reads initialization table stored in external ROM. [Fig. 10] shows initialization routine.



[Fig. 9] Example of Connection with External ROM

* Caution : It covers up to 2K bytes I2C EEPROM. If the I2C EEPROM size is more than 2K bytes then register setting does not operate.



[Fig. 10] Initialization Routine

▶ Access Time of External I2C Master

Because I2C master was designed as a single master and shares SDA/SCL with I2C slave, external I2C master must access to PC7070K after initialization routine as [Fig. 10]. Initialization time depends on the number of registers to be written by external I2C rom. If the number of setting register is 1024d (max.), it will take initialization time about 140ms to be finished after reset. After that, an external I2C master should access to PC7070K.

Access time as below.

Case1 : master enable and with external I2C rom : variable (depend on register numbers, max. 140ms)

Case2 : master enable and without external I2C rom : after about 7.1ms(I2C rom detection time)

Case3 : master disable: always possible

▶ ROM Data Structure for Initialization (I2C ROM)

Address	Contents
0	ABh (Constant) (1)
1	CDh (Constant) (2)
2	reserved(3)
3	reserved(4)
4	reserved(5)
5	reserved(6)
6~8	Common Segment Start
9~11	Common Segment Stop
12~14	TV_mode Segment Start
15~17	TV_mode Segment Stop
18~20	Mirror Segment Start
21~23	Mirror Segment Stop
24~26	Flicker Segment Start
27~29	Flicker Segment Stop
30~32	General Segment Start
33~35	General Segment Stop
36~38	LED Segment Start(7)
39~41	LED Segment Stop(7)

Address	Contents
…	…
Common Start Common Stop	Common Segment
TVmode Start	NTSC
TVmode Stop	PAL
Mirror Start	Mirror=00
	Mirror=01
	Mirror=10
Mirror Stop	Mirror=11
Flicker Start	Flicker=00
	Flicker=01
	Flicker=10
Flicker Stop	Flicker=11
General start	General=000
	General=001
	. . .
General stop	General=111
	LED on
	LED off

[Fig. 11] ROM Data Structure

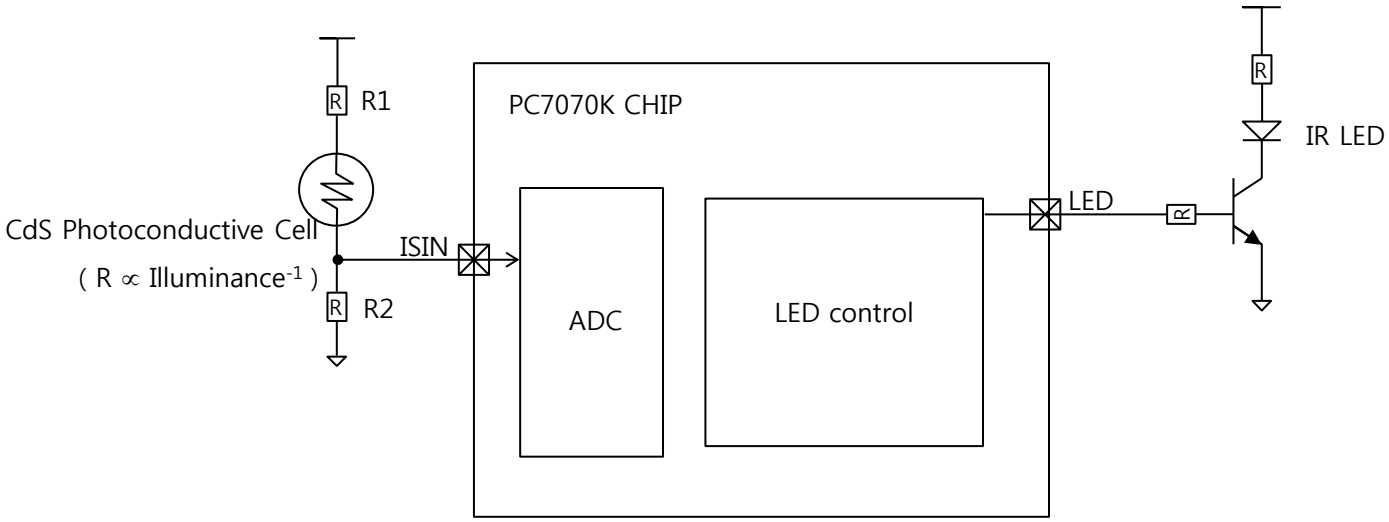
Addresses from 0 to 29d are reserved for Segment Descriptor block. I2C EEPROM data structure for initialization are same.

(1) ~ (2) : ABCDh in address 0-1 are required to detect external ROM.
(3) ~ (5) : These data are not used, but it should be filled with some data. (caution)
(7) : These are not controlled by strap. If exrom_set_en='1'(led_control1[0]), these segments are applied on next field start after led on/off rising or falling.

If some Segment Start address is greater than Segment Stop address, initialization by the segment will be skipped. (User should be set start address < stop address)

▶ *IR LED*

The human eyes can only see visible light between 380~770[nm] wavelength. The image sensors can detect wider wavelength than people. Therefore, the sensors can detect the infra-red light but people can not. As a result, when the sensors detect infra-red light, different colors from the real images come out.



[Fig. 12] IR LED Structure

IR-LED can be controlled by PC7070K which uses analog data from CdS as shown in [Fig. 12]. IR-LED can be controlled automatically by PC7070K without changing registers. This means that additional MICOM (MCU) does not need for the IR-LED control.

1/4 inch NTSC/PAL CMOS Image Sensor with 640 X 480 Pixel Array

▶ 2-wire Serial Interface Description

The registers of PC7070k are written and read through the 2-wire Serial Interface. The PC7070K has 2-wire Serial Interface slave. The PC7070K is controlled by the Register Access Clock (SCL), which is driven by the 2-wire Serial Interface master. Data is transferred into and out of the PC7070K through the Register Access Data (SDA) line. The SCL and SDA lines are pulled up to VDD by a 2kΩ off-chip resistor. Either the slave or master device can pull the lines down. The 2-wire Serial Interface protocol determines which device is allowed to pull the two lines down at any given time.

Start bit

The start bit is defined as a HIGH to LOW transition of the data line while the clock line is HIGH.

Stop bit

The stop bit is defined as a LOW to HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8-bit address of a 2-wire Serial Interface device consists of 7-bit of address and 1-bit of direction. A '0' in the LSB of the address indicates write mode, and a '1' indicates read-mode.

Data bit transfer

One data bit is transferred during each clock pulse. The SCL pulse is provided by the master. The data must be stable during the HIGH period of the SCL. SDA can be only changed when the SCL is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge bit

The receiver generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and receiver indicates an acknowledge bit by pulling the data line low during the acknowledge clock pulse.

No-acknowledge bit

The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

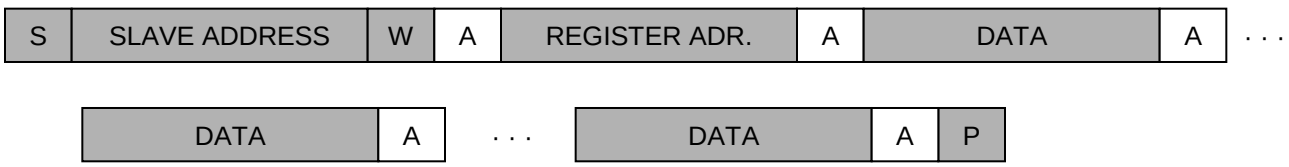
Sequence

A typical read or write sequence begins by the master sending a start bit. After start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request will be a read or a write, where a '0' indicates a write and a '1' indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master. If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The PC7070K uses 8 bit data for its internal registers, thus requiring one 8-bit transfer to write to one register. After 8 bits are transferred, the register address is automatically incremented, so that the next 8 bits are written to the next register address. The master stops writing by sending a start or stop bit. A typical read sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after each 8 bit is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

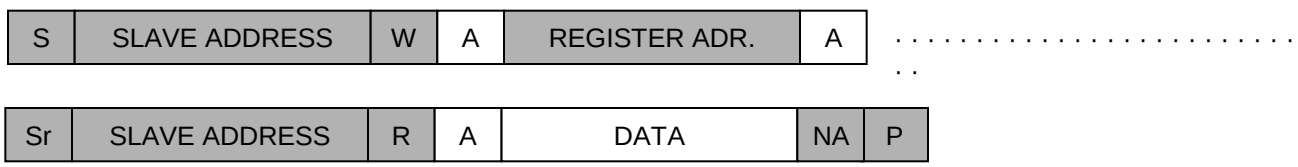
▶ *2-wire Serial Interface Functional Description*

Single Write Mode operation

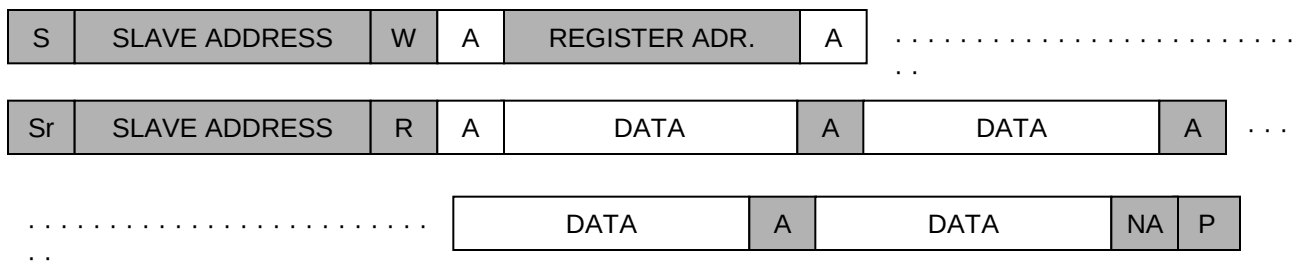
Multiple Write Mode (Register address is increased automatically)[1] operation



Single Read Mode operation



Multiple Read Mode (Register address is increased automatically)[1] operation



From master to slave From slave to master

S: Start condition. Sr : Repeated Start (Start without preceding stop.)

SLAVE ADDRESS: It can be extended 64h to 67h by CADDR pad

write address	**64h**	**66h(default)**
read address	**65h**	**67h(default)**

R/W: Read/Write selection. High = read / LOW = write.

A: Acknowledge bit. NA : No Acknowledge. DATA: 8-bit data. P: Stop condition.

Note 1: Continuous writing or reading without any interrupt increases the register address automatically. If the address is increased above valid register address range, further writing does not affect the chip operation in write mode. Data from invalid registers are undefined in read mode.

▶ Recommended Power-On/Off sequence

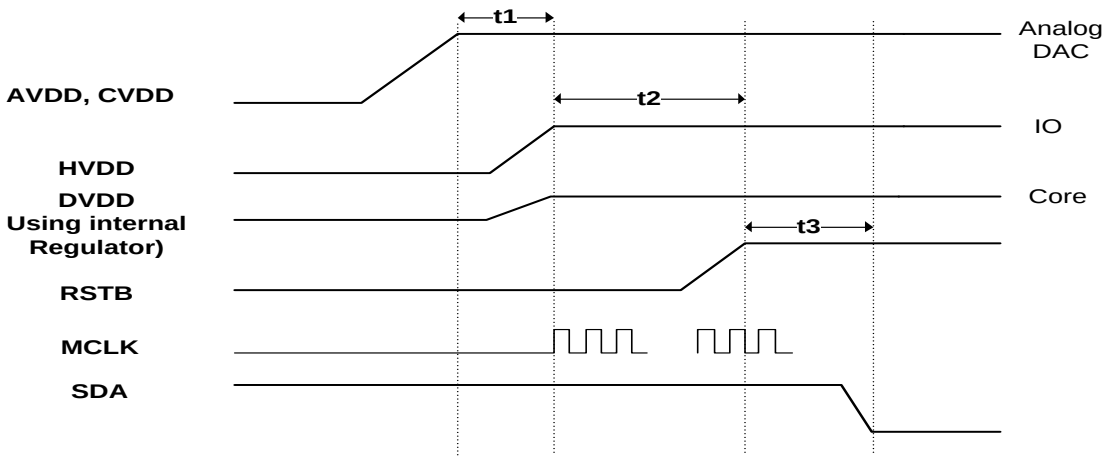
Symbol	Descriptions	Min	Typ	Max	Unit	Remark
t1	From AVDD,CVDD rising to HVDD rising	0			ns	
t2	Sensor reset time	8*mclk				
t3(*)	Initialize time after releasing Reset : Reading internal or external ROM out	8.0(0)		280(0)	ms	Depend on the number of registers
t4	From AVDD,CVDD falling to HVDD falling	0			ns	

•t3 is just applied to strap_master(VSYNC)='1

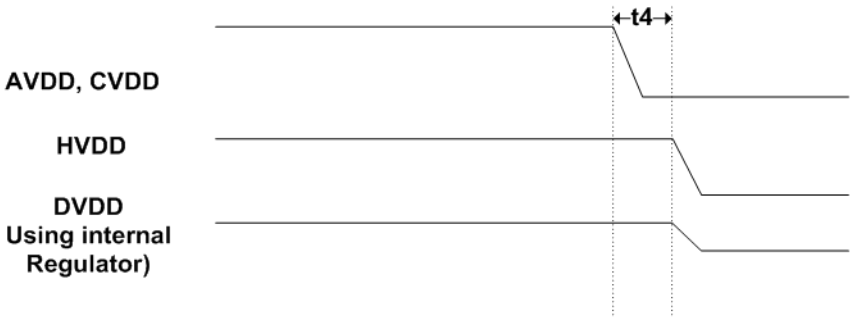
•If user use a strap_master(VSYNC)='0', then t3 is 0ms.

[Table 9] Recommended Power-On/Off sequence

※ Power-On Sequence



※ Power-down Sequence



1/4 inch NTSC/PAL CMOS Image Sensor with 640 X 480 Pixel Array

▶ Register Tables – Group A

GROUP A									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
0	00	DeviceID_H	0	00	00000000	RO	0	0	device ID
1	01	DeviceID_L	0	00	00000000	RO	0	0	
2	02	RevNumber	0	00	00000000	RO	0	0	revision number
3	03	bank	0	00	xxxx0000	RW	5	0	Register group selector
4	04	chip_mode	u	u	uuuuuuuu	RW	7	aev	chip mode selection(NTSC, PAL)
5	05	mirror	u	u	uuuuuuuu	RW	7	aev	Mirror
6	06	framewidth_h	u	u	uuuuuuuu	RW	7	aev	Framewidth
7	07	framewidth_l	u	u	uuuuuuuu	RW	7	aev	
8	08	fd_fheight_a_h	2	02	xxx00010	RW	6	aev	Frameheight
9	09	fd_fheight_a_l	u	u	uuuuuuuu	RW	7	aev	
10	0A	fd_fheight_b_h	2	02	xxx00010	RW	6	aev	
11	0B	fd_fheight_b_l	u	u	uuuuuuuu	RW	7	aev	
20	14	vsyncstartrow_f0_h	0	00	xxx00000	RW	6	aev	Vsync generation
21	15	vsyncstartrow_f0_l	23	17	00010111	RW	6	aev	
22	16	vsyncstoprow_f0_h	1	01	xxx00001	RW	6	aev	
23	17	vsyncstoprow_f0_l	u	u	uuuuuuuu	RW	7	aev	
24	18	vsyncstartrow_f1_h	1	01	xxx00001	RW	6	aev	
25	19	vsyncstartrow_f1_l	u	u	uuuuuuuu	RW	7	aev	
26	1A	vsyncstoprow_f1_h	2	02	xxx00010	RW	6	aev	
27	1B	vsyncstoprow_f1_l	u	u	uuuuuuuu	RW	7	aev	
28	1C	vsynccolumn_h	0	00	xxxx0000	RW	5	0	
29	1D	vsynccolumn_l	2	02	00000010	RW	5	0	
36	24	softreset	0	00	xxxxxxx0	RW	5	0	Soft reset
37	25	clkdiv	32	20	xx100000	RW	6	aev	Clock divider
39	27	pad_control1	102	66	01100110	RW	5	0	Pad control
40	28	pad_control2	0	00	00000000	RW	5	0	Pad control
41	29	pad_control3	0	00	00000000	RW	5	0	Pad control
42	2A	pad_control4	0	00	00000000	RW	5	0	Pad control
45	2D	pad_control7	0	00	00000000	RW	5	0	Pad control
46	2E	pad_control8	0	00	00000000	RW	5	0	Pad control
47	2F	pad_control9	0	00	00000000	RW	5	0	Pad control
48	30	strap_control	255	FF	11111111	RW	5	0	Strap control
51	33	pixelbias	8	08	xxxx1000	RW	5	0	Pixel bias
52	34	compbias	5	05	xxx00101	RW	5	0	Comparator bias
79	4F	flicker_control1	u	u	uuuuuuuu	RW	5	0	Flicker control
89	59	fd_period_a_h	u	u	uuuuuuuu	RW	5	0	Flicker period for A state
90	5A	fd_period_a_m	u	u	uuuuuuuu	RW	5	0	
91	5B	fd_period_a_l	u	u	uuuuuuuu	RW	5	0	
92	5C	fd_period_b_h	1	01	00000001	RW	5	0	Flicker period for B state
93	5D	fd_period_b_m	u	u	uuuuuuuu	RW	5	0	
94	5E	fd_period_b_l	u	u	uuuuuuuu	RW	5	0	
123	7B	led_control1	1	01	00000001	RW	5	0	Auto LED control
124	7C	led_lvth1	0	00	00000000	RW	5	0	Led control level th.1
125	7D	led_lvth2	0	00	00000000	RW	5	0	Led control level th.2
126	7E	led_frame	128	80	10000000	RW	5	0	Led frame control
162	A2	spi_osd_control	u	u	uuuuuuuu	RW	5	0	SPI OSD control

▶ Register Tables – Group B

GROUP B									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
256	00	DeviceID_H	0	00	00000000	RO	0	0	device ID
257	01	DeviceID_L	0	00	00000000	RO	0	0	
258	02	RevNumber	0	00	00000000	RO	0	0	revision number
259	03	bank	0	00	00000000	RO	5	0	Register group selector
444	BC	inttime_h	1	01	00000001	RW	6	aev	Integration time (line)
445	BD	inttime_m	64	40	01000000	RW	6	aev	
446	BE	inttime_l	0	00	00000000	RW	6	aev	Integration time (column)
447	BF	globalgain	0	00	00000000	RW	6	aev	Analog gain
448	C0	digitalgain	64	40	01000000	RW	6	aev	Digital gain
471	D7	real_led_data	0	00	00000000	RO	0	0	Current CdS data

▶ Register Tables – Group C

GROUP C									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
512	00	DeviceID_H	0	00	00000000	RO	0	0	device ID
513	01	DeviceID_L	0	00	00000000	RO	0	0	
514	02	RevNumber	0	00	00000000	RO	0	0	revision number
515	03	bank	0	00	00000000	RO	5	0	Register group selector
516	04	isp_func_0	247	F7	11110111	RW	6	aev	Isp function control
517	05	isp_func_1	254	FE	11111110	RW	6	aev	Isp function control
526	0E	lens_scale	81	51	01010001	RW	5	0	Lens shading compensation scale control
527	0F	lens_gainr	0	00	00000000	RW	6	aev	Lens shading compensation R gain
528	10	lens_gaing1	2	02	00000010	RW	6	aev	Lens shading compensation G1 gain
529	11	lens_gaing2	2	02	00000010	RW	6	aev	Lens shading compensation G2 gain
530	12	lens_gainb	0	00	00000000	RW	6	aev	Lens shading compensation B gain
531	13	lens_x	0	00	00000000	RW	5	0	Lens shading compensation center control
532	14	lens_y	0	00	00000000	RW	5	0	
548	24	edge_gain_ref0	32	20	00100000	RW	5	0	Edge gain fitting control
549	25	edge_gain_ref1	32	20	00100000	RW	5	0	
550	26	edge_gain_ref2	32	20	00100000	RW	5	0	
551	27	edge_gain	32	20	00100000	RW	6	aev	
563	33	ccr_m11	43	2B	00101011	RW	5	0	Color correction matrix value
564	34	ccr_m12	138	8A	10001010	RW	5	0	
565	35	ccr_m13	129	81	10000001	RW	5	0	
566	36	ccr_m21	138	8A	10001010	RW	5	0	
567	37	ccr_m22	50	32	00110010	RW	5	0	
568	38	ccr_m23	136	88	10001000	RW	5	0	
569	39	ccr_m31	131	83	10000011	RW	5	0	
570	3A	ccr_m32	156	9C	10011100	RW	5	0	
571	3B	ccr_m33	63	3F	00111111	RW	5	0	

(Group C – continued)

▶ Register Tables – Group C

GROUP C									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
573	3D	ygm1_y0	0	00	00000000	RW	5	0	Y gamma1 coefficient
574	3E	ygm1_y1	3	03	00000011	RW	5	0	
575	3F	ygm1_y2	12	0C	00001100	RW	5	0	
576	40	ygm1_y3	25	19	00011001	RW	5	0	
577	41	ygm1_y4	38	26	00100110	RW	5	0	
578	42	ygm1_y5	63	3F	00111111	RW	5	0	
579	43	ygm1_y6	82	52	01010010	RW	5	0	
580	44	ygm1_y7	110	6E	01101110	RW	5	0	
581	45	ygm1_y8	130	82	10000010	RW	5	0	
582	46	ygm1_y9	161	A1	10100001	RW	5	0	
583	47	ygm1_y10	185	B9	10111001	RW	5	0	
584	48	ygm1_y11	206	CE	11001110	RW	5	0	
585	49	ygm1_y12	224	E0	11100000	RW	5	0	
586	4A	ygm1_y13	240	F0	11110000	RW	5	0	
587	4B	ygm1_y14	255	FF	11111111	RW	5	0	
588	4C	ygm2_y0	0	00	00000000	RW	5	0	Y gamma2 coefficient
589	4D	ygm2_y1	11	0B	00001011	RW	5	0	
590	4E	ygm2_y2	23	17	00010111	RW	5	0	
591	4F	ygm2_y3	34	22	00100010	RW	5	0	
592	50	ygm2_y4	46	2E	00101110	RW	5	0	
593	51	ygm2_y5	64	40	01000000	RW	5	0	
594	52	ygm2_y6	80	50	01010000	RW	5	0	
595	53	ygm2_y7	110	6E	01101110	RW	5	0	
596	54	ygm2_y8	136	88	10001000	RW	5	0	
597	55	ygm2_y9	174	AE	10101110	RW	5	0	
598	56	ygm2_y10	202	CA	11001010	RW	5	0	
599	57	ygm2_y11	220	DC	11011100	RW	5	0	
600	58	ygm2_y12	236	EC	11101100	RW	5	0	
601	59	ygm2_y13	246	F6	11110110	RW	5	0	
602	5A	ygm2_y14	255	FF	11111111	RW	5	0	
603	5B	cgm1_y0	0	00	00000000	RW	5	0	RGB gamma1 coefficient
604	5C	cgm1_y1	11	0B	00001011	RW	5	0	
605	5D	cgm1_y2	23	17	00010111	RW	5	0	
606	5E	cgm1_y3	34	22	00100010	RW	5	0	
607	5F	cgm1_y4	46	2E	00101110	RW	5	0	
608	60	cgm1_y5	64	40	01000000	RW	5	0	
609	61	cgm1_y6	80	50	01010000	RW	5	0	
610	62	cgm1_y7	110	6E	01101110	RW	5	0	
611	63	cgm1_y8	136	88	10001000	RW	5	0	
612	64	cgm1_y9	174	AE	10101110	RW	5	0	
613	65	cgm1_y10	202	CA	11001010	RW	5	0	
614	66	cgm1_y11	220	DC	11011100	RW	5	0	
615	67	cgm1_y12	236	EC	11101100	RW	5	0	
616	68	cgm1_y13	246	F6	11110110	RW	5	0	
617	69	cgm1_y14	255	FF	11111111	RW	5	0	

(Group C – continued)

▶ Register Tables – Group C

GROUP C									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
618	6A	cgm2_y0	0	00	00000000	RW	5	0	RGB gamma2 coefficient
619	6B	cgm2_y1	11	0B	00001011	RW	5	0	
620	6C	cgm2_y2	23	17	00010111	RW	5	0	
621	6D	cgm2_y3	34	22	00100010	RW	5	0	
622	6E	cgm2_y4	46	2E	00101110	RW	5	0	
623	6F	cgm2_y5	64	40	01000000	RW	5	0	
624	70	cgm2_y6	80	50	01010000	RW	5	0	
625	71	cgm2_y7	110	6E	01101110	RW	5	0	
626	72	cgm2_y8	136	88	10001000	RW	5	0	
627	73	cgm2_y9	174	AE	10101110	RW	5	0	
628	74	cgm2_y10	202	CA	11001010	RW	5	0	
629	75	cgm2_y11	220	DC	11011100	RW	5	0	
630	76	cgm2_y12	236	EC	11101100	RW	5	0	
631	77	cgm2_y13	246	F6	11110110	RW	5	0	
632	78	cgm2_y14	255	FF	11111111	RW	5	0	
640	80	cs11	37	25	00100101	RW	6	aev	Color saturation matrix value
641	81	cs12	0	00	00000000	RW	6	aev	
642	82	cs21	0	00	00000000	RW	6	aev	
643	83	cs22	37	25	00100101	RW	6	aev	
660	94	ycontrast	64	40	01000000	RW	6	aev	Y contrast
661	95	ybrightness_ref0	0	00	00000000	RW	5	0	Y brightness fitting control
662	96	ybrightness_ref1	0	00	00000000	RW	5	0	
663	97	ybrightness_ref2	0	00	00000000	RW	5	0	
664	98	ybrightness	0	00	00000000	RW	6	aev	
691	B3	ae_fwx1_h	0	00	xxxxxx00	RW	5	0	AE full window X start position
692	B4	ae_fwx1_l	1	01	00000001	RW	5	0	
693	B5	ae_fwx2_h	2	02	xxxxxx10	RW	5	0	AE full window X stop position
694	B6	ae_fwx2_l	128	80	10000000	RW	5	0	
695	B7	ae_fwy1_h	0	00	xxxxxx00	RW	5	0	AE full window Y start position
696	B8	ae_fwy1_l	1	01	00000001	RW	5	0	
697	B9	ae_fwy2_h	1	01	xxxxxx01	RW	5	0	AE full window Y stop position
698	BA	ae_fwy2_l	224	E0	11100000	RW	5	0	
699	BB	ae_cwx1_h	0	00	xxxxxx00	RW	5	0	AE center window X start position
700	BC	ae_cwx1_l	214	D6	11010110	RW	5	0	
701	BD	ae_cwx2_h	1	01	xxxxxx01	RW	5	0	AE center window X stop position
702	BE	ae_cwx2_l	171	AB	10101011	RW	5	0	
703	BF	ae_cwy1_h	0	00	xxxxxx00	RW	5	0	AE center window Y start position
704	C0	ae_cwy1_l	161	A1	10100001	RW	5	0	
705	C1	ae_cwy2_h	1	01	xxxxxx01	RW	5	0	AE center window Y stop position
706	C2	ae_cwy2_l	64	40	01000000	RW	5	0	
707	C3	ae_xaxis_h	1	01	xxxxxx01	RW	5	0	AE window X axis
708	C4	ae_xaxis_l	65	41	01000001	RW	5	0	
709	C5	ae_yaxis_h	0	00	xxxxxx00	RW	5	0	AE window Y axis
710	C6	ae_yaxis_l	241	F1	11110001	RW	5	0	
711	C7	awb_wx1_h	0	00	xxxxxx00	RW	5	0	AWB window X start position
712	C8	awb_wx1_l	1	01	00000001	RW	5	0	
713	C9	awb_wx2_h	2	02	xxxxxx10	RW	5	0	AWB window X stop position
714	CA	awb_wx2_l	128	80	10000000	RW	5	0	
715	CB	awb_wy1_h	0	00	xxxxxx00	RW	5	0	AWB window Y start position
716	CC	awb_wy1_l	1	01	00000001	RW	5	0	
717	CD	awb_wy2_h	1	01	xxxxxx01	RW	5	0	AWB window Y stop position
718	CE	awb_wy2_l	224	E0	11100000	RW	5	0	

▶ Register Tables – Group D

GROUP D									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
768	00	DeviceID_H	0	00	00000000	RO	0	0	device ID
769	01	DeviceID_L	0	00	00000000	RO	0	0	
770	02	RevNumber	0	00	00000000	RO	0	0	revision number
771	03	bank	0	00	00000000	RO	5	0	Register group selector
772	04	cs11_a	40	28	00101000	RW	5	0	Color saturation matrix fitting reference
773	05	cs12_a	0	00	00000000	RW	5	0	
774	06	cs21_a	0	00	00000000	RW	5	0	
775	07	cs22_a	40	28	00101000	RW	5	0	
776	08	cs11_b	36	24	00100100	RW	5	0	
777	09	cs12_b	0	00	00000000	RW	5	0	
778	0A	cs21_b	0	00	00000000	RW	5	0	
779	0B	cs22_b	40	28	00101000	RW	5	0	
780	0C	cs11_c	32	20	00100000	RW	5	0	
781	0D	cs12_c	0	00	00000000	RW	5	0	
782	0E	cs21_c	0	00	00000000	RW	5	0	
783	0F	cs22_c	32	20	00100000	RW	5	0	
784	10	axis_a	58	3A	00111010	RW	5	0	CS matrix / lens gain fitting reference
785	11	axis_b	84	54	01010100	RW	5	0	
786	12	axis_c	89	59	01011001	RW	5	0	
787	13	user_cs	56	38	00111000	RW	5	0	User CS gain
795	1B	wb_rgain_h	0	00	00000000	RW	6	aev	Normalized white balance gain
796	1C	wb_rgain_l	93	5D	01011101	RW	6	aev	
797	1D	wb_ggain_h	0	00	00000000	RW	6	aev	
798	1E	wb_ggain_l	64	40	01000000	RW	6	aev	
799	1F	wb_bgain_h	0	00	00000000	RW	6	aev	
800	20	wb_bgain_l	94	5E	01011110	RW	6	aev	
854	56	dark_ccr0	0	00	00000000	RW	5	0	Dark color correction fitting control
855	57	dark_ccr1	128	80	10000000	RW	5	0	
856	58	dark_ccr2	255	FF	11111111	RW	5	0	
857	59	dark_ccr	0	00	00000000	RW	6	aev	
869	65	dark_ec_pth0	4	04	00000100	RW	5	0	Dark edge clamp plus threshold filter control
870	66	dark_ec_pth1	80	50	01010000	RW	5	0	
871	67	dark_ec_pth2	160	A0	10100000	RW	5	0	
872	68	dark_ec_pth	4	04	00000100	RW	6	aev	
873	69	dark_ec_mth0	4	04	00000100	RW	5	0	Dark edge clamp minus threshold filter control
874	6A	dark_ec_mth1	64	40	01000000	RW	5	0	
875	6B	dark_ec_mth2	128	80	10000000	RW	5	0	
876	6C	dark_ec_mth	4	04	00000100	RW	6	aev	
887	77	dark_dc0	0	00	00000000	RW	5	0	de-color dark filter fitting control
888	78	dark_dc1	0	00	00000000	RW	5	0	
889	79	dark_dc2	6	06	00000110	RW	5	0	
890	7A	dark_dc	0	00	00000000	RW	6	aev	
919	97	y_cont_th2_ref0	128	80	10000000	RW	5	0	Dark y contrast th2 fitting control
920	98	y_cont_th2_ref1	128	80	10000000	RW	5	0	
921	99	y_cont_th2_ref2	128	80	10000000	RW	5	0	
922	9A	y_cont_th2	128	80	10000000	RW	6	aev	
923	9B	y_cont_slope2_ref0	64	40	01000000	RW	5	0	Dark y contrast slope2 fitting control
924	9C	y_cont_slope2_ref1	64	40	01000000	RW	5	0	
925	9D	y_cont_slope2_ref2	64	40	01000000	RW	5	0	
926	9E	y_cont_slope2	64	40	01000000	RW	6	aev	

1/4 inch NTSC/PAL CMOS Image Sensor with 640 X 480 Pixel Array

▶ Register Tables – Group E

GROUP E									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1024	00	DeviceID_H	0	00	00000000	RO	0	0	device ID
1025	01	DeviceID_L	0	00	00000000	RO	0	0	
1026	02	RevNumber	0	00	00000000	RO	0	0	revision number
1027	03	bank	0	00	00000000	RO	5	0	Register group selector
1028	04	auto_control_1	152	98	10011000	RW	6	autov	Auto control
1042	12	expfrmh_h	2	02	00000010	RW	5	0	AE reference
1043	13	expfrmh_l	u	u	uuuuuuuu	RW	5	0	
1044	14	midfrmheight_h	2	02	00000010	RW	5	0	
1045	15	midfrmheight_l	u	u	uuuuuuuu	RW	5	0	
1046	16	maxfrmheight_h	2	02	00000010	RW	5	0	
1047	17	maxfrmheight_l	u	u	uuuuuuuu	RW	5	0	
1048	18	minexp_h	0	00	00000000	RW	5	0	
1049	19	minexp_m	0	00	00000000	RW	5	0	
1050	1A	minexp_l	12	0C	00001100	RW	5	0	
1051	1B	midexp_t	1	01	00000001	RW	5	0	
1052	1C	midexp_h	129	81	10000001	RW	5	0	
1053	1D	midexp_m	128	80	10000000	RW	5	0	
1054	1E	maxexp_t	3	03	00000011	RW	5	0	
1055	1F	maxexp_h	3	03	00000011	RW	5	0	
1056	20	maxexp_m	0	00	00000000	RW	5	0	
1058	22	ext_inttime_h	0	00	00000000	RW	6	autov	Manual integration time @ external AE mode
1059	23	ext_inttime_m	128	80	10000000	RW	6	autov	
1060	24	ext_inttime_l	0	00	00000000	RW	6	autov	
1061	25	ext_glbg_h	1	01	00000001	RW	6	autov	Manual analog gain @ external AE mode
1062	26	ext_glbg_l	0	00	00000000	RW	6	autov	
1063	27	exposure_t	0	00	00000000	RW	6	autov	Exposure
1064	28	exposure_h	1	01	00000001	RW	6	autov	
1065	29	exposure_m	64	40	01000000	RW	6	autov	
1066	2A	exposure_l	0	00	00000000	RW	6	autov	
1072	30	ae_weight1	8	08	xx001000	RW	5	0	AE weight peripheral
1073	31	ae_weight2	8	08	xx001000	RW	5	0	
1074	32	ae_weight3	8	08	xx001000	RW	5	0	
1075	33	ae_weight4	8	08	xx001000	RW	5	0	
1076	34	ae_weightc	8	08	xx001000	RW	5	0	AE weight center
1081	39	ymean_h	0	00	00000000	RW	5	0	Y mean
1082	3A	ymean_l	128	80	10000000	RW	5	0	
1083	3B	max_yt1	160	A0	10100000	RW	6	autov	Min / max ytarget control reference
1084	3C	max_yt2	128	80	10000000	RW	6	autov	
1085	3D	min_yt1	120	78	01111000	RW	6	autov	
1086	3E	min_yt2	120	78	01111000	RW	6	autov	
1096	48	ae_up_speed	8	08	00001000	RW	6	autov	AE upside speed
1097	49	ae_down_speed	8	08	00001000	RW	6	autov	AE downside speed
1098	4A	ae_lock	16	10	00010000	RW	6	autov	AE lock range

(Group E – continued)

1/4 inch NTSC/PAL CMOS Image Sensor with 640 X 480 Pixel Array

▶ Register Tables – Group E

GROUP E									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1128	68	rg_ratio_a	128	80	10000000	RW	5	0	Target awb ratio fitting reference
1129	69	bg_ratio_a	128	80	10000000	RW	5	0	
1130	6A	rg_ratio_b	128	80	10000000	RW	5	0	
1131	6B	bg_ratio_b	128	80	10000000	RW	5	0	
1132	6C	rg_ratio_c	128	80	10000000	RW	5	0	
1133	6D	bg_ratio_c	128	80	10000000	RW	5	0	
1134	6E	ratio_axis_a	58	3A	00111010	RW	5	0	
1135	6F	ratio_axis_b	84	54	01010100	RW	5	0	
1136	70	ratio_axis_c	89	59	01011001	RW	5	0	
1137	71	awb_rgratio	128	80	10000000	RW	5	0	AWB RG ratio control
1138	72	awb_bgratio	128	80	10000000	RW	5	0	AWB BG ratio control
1139	73	awb_lock	16	10	00010000	RW	5	0	AWB lock range
1140	74	awb_speed	4	04	00000100	RW	5	0	AWB speed
1141	75	awb_rgain_min	0	00	00000000	RW	5	0	AWB gain clamping control
1142	76	awb_rgain_max	255	FF	11111111	RW	5	0	
1143	77	awb_bgain_min	0	00	00000000	RW	5	0	
1144	78	awb_bgain_max	255	FF	11111111	RW	5	0	
1177	99	totalgain_h	0	00	00000000	RW	6	autov	Total gain
1178	9A	totalgain_l	1	01	00000001	RW	6	autov	

1/4 inch NTSC/PAL CMOS Image Sensor with 640 X 480 Pixel Array

▶ Register Tables – Group F

GROUP E									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1280	00	DeviceID_H	0	00	00000000	RO	0	0	device ID
1281	01	DeviceID_L	0	00	00000000	RO	0	0	
1282	02	RevNumber	0	00	00000000	RO	0	0	revision number
1283	03	bank	0	00	00000000	RO	5	0	Register group selector
1284	04	pg_control0	9	09	00001001	RW	6	aev	Embedded parking guide line control
1288	08	pg_yt	127	7F	01111111	RW	6	aev	
1289	09	pg_y1	115	73	01110011	RW	6	aev	
1290	0A	pg_y2	2	02	00000010	RW	6	aev	
1291	0B	pg_y3	8	08	00001000	RW	6	aev	
1292	0C	pg_y4	15	0F	00001111	RW	6	aev	
1293	0D	pg_y5	25	19	00011001	RW	6	aev	
1294	0E	pg_y6	37	25	00100101	RW	6	aev	
1295	0F	pg_y7	40	28	00101000	RW	6	aev	
1296	10	pg_y8	56	38	00111000	RW	6	aev	
1297	11	pg_y9	78	4E	01001110	RW	6	aev	
1298	12	pg_y10	82	52	01010010	RW	6	aev	
1299	13	pg_a	143	8F	10001111	RW	6	aev	
1300	14	pg_b	100	64	01100100	RW	6	aev	
1301	15	pg_c	191	BF	10111111	RW	6	aev	
1302	16	pg_d	7	07	00000111	RW	6	aev	
1303	17	pg_e	12	0C	00001100	RW	6	aev	
1304	18	pg_f	21	15	00010101	RW	6	aev	Embedded parking guide line control
1305	19	pg_line1	33	21	00100001	RW	6	aev	
1306	1A	pg_line2	35	23	00100011	RW	6	aev	
1307	1B	pg_line3	36	24	00100100	RW	6	aev	
1308	1C	pg_line4	70	46	01000110	RW	6	aev	
1309	1D	pg_line5	72	48	01001000	RW	6	aev	
1310	1E	pg_line6	66	42	01000010	RW	6	aev	
1311	1F	pg_line7	75	4B	01001011	RW	6	aev	
1312	20	pg_line8	113	71	01110001	RW	6	aev	
1313	21	pg_line9	99	63	01100011	RW	6	aev	
1314	22	pg_line10	116	74	01110100	RW	6	aev	
1315	23	pg_center_h	1	01	xxxxxx01	RW	6	aev	
1316	24	pg_center_l	104	68	01101000	RW	6	aev	
1317	25	pg_l_type_h	1	01	xxxxxx01	RW	6	aev	
1318	26	pg_l_type_l	33	21	00100001	RW	6	aev	
1319	27	pg_hl_en_h	0	00	xxxxxx00	RW	6	aev	
1320	28	pg_hl_en_l	0	00	00000000	RW	6	aev	
1435	9B	blink_frame	0	00	00000000	RW	5	0	OSD blink control
1437	9D	spi_osd_bndry	0	00	00000000	RW	5	0	OSD boundary

1/4 inch NTSC/PAL CMOS Image Sensor with 640 X 480 Pixel Array

▶ Register Tables – Group G

GROUP E									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1536	00	DeviceID_H	0	00	00000000	RO	0	0	device ID
1537	01	DeviceID_L	0	00	00000000	RO	0	0	
1538	02	RevNumber	0	00	00000000	RO	0	0	revision number
1539	03	bank	0	00	00000000	RO	5	0	Register group selector
1540	04	sync_blankEAV_f0	182	B6	10110110	RW	5	0	Blank EAV for field0 of CCIR656 data or blank EAV for frame data
1541	05	sync_blankSAV_f0	171	AB	10101011	RW	5	0	Blank SAV for field0 of CCIR656 data or blank SAV for frame data
1542	06	sync_activeEAV_f0	157	9D	10011101	RW	5	0	Active EAV for field0 of CCIR656 data or active EAV for frame data
1543	07	sync_activeSAV_f0	128	80	10000000	RW	5	0	Active SAV for field0 of CCIR656 data or active SAV for frame data
1544	08	sync_blankEAV_f1	241	F1	11110001	RW	5	0	blank EAV for field1 of CCIR656 data
1545	09	sync_blankSAV_f1	236	EC	11101100	RW	5	0	blank SAV for field1 of CCIR656 data
1546	0A	sync_activeEAV_f1	218	DA	11011010	RW	5	0	Active EAV for field1 of CCIR656 data
1547	0B	sync_activeSAV_f1	199	C7	11000111	RW	5	0	Active SAV for field1 of CCIR656 data
1548	0C	sync_CCIR_FF	255	FF	11111111	RW	5	0	CCIR data format
1549	0D	sync_CCIR_00	0	00	00000000	RW	5	0	
1550	0E	sync_CCIR_80	128	80	10000000	RW	5	0	
1551	0F	sync_CCIR_10	16	10	00010000	RW	5	0	
1560	18	osd_opac	16	10	xxx10000	RW	5	0	OSD transparency
1562	1A	palette_1_y	144	90	10010000	RW	5	0	Palette_1
1563	1B	palette_1_cb	53	35	00110101	RW	5	0	
1564	1C	palette_1_cr	34	22	00100010	RW	5	0	
1565	1D	palette_2_y	210	D2	11010010	RW	5	0	Palette_2
1566	1E	palette_2_cb	16	10	00010000	RW	5	0	
1567	1F	palette_2_cr	146	92	10010010	RW	5	0	
1568	20	palette_3_y	81	51	01010001	RW	5	0	Palette_3
1569	21	palette_3_cb	90	5A	01011010	RW	5	0	
1570	22	palette_3_cr	240	F0	11110000	RW	5	0	
1571	23	palette_4_y	16	10	00010000	RW	5	0	Palette_4
1572	24	palette_4_cb	128	80	10000000	RW	5	0	
1573	25	palette_4_cr	128	80	10000000	RW	5	0	
1693	9D	enc_control1	0	00	00000000	RW	5	0	Encoder control
1705	A9	setup_w	7	07	xxx00111	RW	5	0	Setup time width
1706	AA	hsync_p_toffset	0	00	xxx00000	RW	5	0	Stop point of hsync
1707	AB	burst_duration	0	00	00000000	RW	5	0	Burst duration
1708	AC	burst_slope_step	56	38	00111000	RW	5	0	
1709	AD	l_blank_start	0	00	00000000	RW	5	0	Line blanking interval
1710	AE	l_blank_stop	0	00	00000000	RW	5	0	
1711	AF	sync_rising	1	01	xxxx0001	RW	5	0	horizontal rising time control of composite signal
1712	B0	resol_gain	8	08	00001000	RW	5	0	Resolution enhance gain
1719	B7	enc_mode	u	u	uuuuuuuu	RW	5	0	Encoder mode
1720	B8	enc_sync	16	10	00010000	RW	5	0	Encoder sync level
1721	B9	enc_blankH	0	00	00000000	RW	5	0	Encoder blank level
1722	BA	enc_blankL	u	u	uuuuuuuu	RW	5	0	
1723	BB	enc_pedestal	u	u	uuuuuuuu	RW	5	0	Encoder pedestal
1724	BC	enc_burst	u	u	uuuuuuuu	RW	5	0	Burst amplitude

(Group G – continued)

1/4 inch NTSC/PAL CMOS Image Sensor with 640 X 480 Pixel Array

▶ Register Tables – Group G

GROUP E									
#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1725	BD	enc_Ygain	u	u	uuuuuuuu	RW	5	0	Y convergence gain from YCbCr to YUV
1726	BE	enc_Ugain	u	u	uuuuuuuu	RW	5	0	U convergence gain from YCbCr to YUV
1727	BF	enc_Vgain	u	u	uuuuuuuu	RW	5	0	V convergence gain from YCbCr to YUV
1728	C0	enc_Yrange_H	3	03	xxxxx011	RW	5	0	Max. luminance
1729	C1	enc_Yrange_L	32	20	00100000	RW	5	0	
1730	C2	enc_Crange_H	1	01	xxxxx001	RW	5	0	Max. amplitudes of chrominance
1731	C3	enc_Crange_L	u	u	uuuuuuuu	RW	5	0	
1732	C4	enc_chroma_max_H	3	03	xxxxx011	RW	5	0	Maximum chrominance of composite output
1733	C5	enc_chroma_max_L	u	u	uuuuuuuu	RW	5	0	
1734	C6	enc_chroma_min_H	0	00	xxxxx000	RW	5	0	Minimum chrominance of composite output
1735	C7	enc_chroma_min_L	u	u	uuuuuuuu	RW	5	0	
1766	E6	burst_toffset	0	00	00000000	RW	5	0	Burst time +/- offset
1771	EB	encdat_rising	1	01	xxxx0001	RW	5	0	edge of the line blanking pulse rising time control
1772	EC	enc_scfreq	u	u	uuuuuuuu	RW	5	0	Subcarrier frequency selection for which TV mode

▶ Register Tables (Detailed) : Group A

< Group A >

Register names are written in *slanted* characters. To differentiate between decimal, binary, and hexa numbers, (d, b, and h) are appended. The sensor should be reset by RSTB pin set low, after power is up, for at least 16 master clock periods. This will initialize all of the registers to their default values. Default values of 'U' are wire-strapping registers.

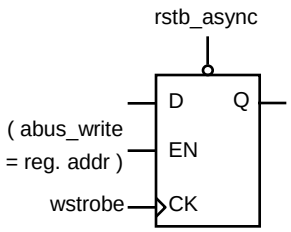
There are two register type.

1. Available Read Only (indicator is RO).
2. Available Read and Write (indicator is RW).

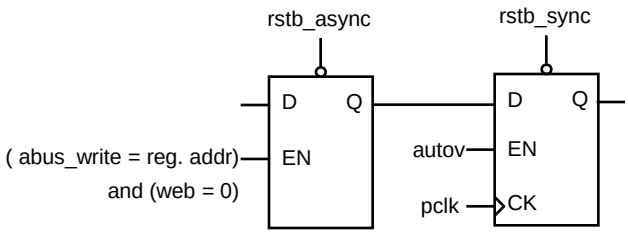
In addition, RW type register can be grouped by stage. There are 3 register stage.

1. 1 stage register (indicator is [5, 0]).
2. 2 stage register which is updated at auto vsync falling edge (indicator is [6, autov]).
3. 2 stage register which is updated at ae vsync falling edge (indicator is [6, aev]).
4. 2 stage register which is updated at ae vsync falling edge (indicator is [7, aev]) → this is 2 flip-flop structure.

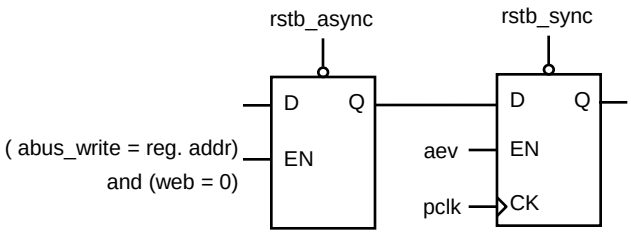
Below figure shows block diagram by register stage.



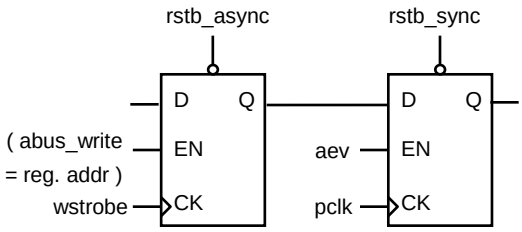
1. [1 stage register]



2. [2 stage register @ autov]



3. [2 stage register @ aev]



4. [2 stage register @ aev]

Where, abus_write means user input address by 2-wire serial interface. wstrobe and web is generated by SSCL pin. pclk means pixel clock for core. aev means ae vsync falling edge. autov means auto vsync falling edge. For more information of ae vsync and auto vsync, please refer to Reg. C-ACh~B1h.

< Group A >

< Group A >

(0~3) DeviceID, RevNumber, Register Selector

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
0	00	DeviceID_H	112	70	00000000	RO	0	0	device ID
1	01	DeviceID_L	48	30	00000000	RO	0	0	
2	02	RevNumber	0	00	00000000	RO	0	0	revision number
3	03	bank	0	00	xxxx0000	RW	5	0	Register group selector

▷ **DeviceID, RevNumber, Register Selector**

PC7070K device ID, reversion number, Register Selector.

Register Group A(00h) / B(01h) / C(02h) / D(03h) / E(04h) / F(05h) / G(06h)

(4) Chip mode

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
4	04	chip_mode	u	u	uuuuuuuu	RW	7	aev	chip mode selection(NTSC, PAL)

register name : chip_mdoe								
register #	bit#	name	default	**U**	default(h)	**UU**	default(b)	**xxxxxxuu**
04d (04h)	7	x	0	Reserved				
	6	x	0	Reserved				
	5	x	0	Reserved				
	4	x	0	Reserved				
	3	x	0	Reserved				
	2	x	0	Reserved				
	1	chip_mode	U	Chip mode selection 00b - NTSC, (M)PAL 01b - PAL				
	0		U					

▷ **chip_mode**

default value : U wire-strapping register

Chip mode selection

The default value of this register is changed by wire-strapping. After changed wire-strapping, the register can be set with other values through SCL and SDA.

< Group A >

< Group A >

(5) Mirror

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
5	05	mirror	u	u	uuuuuuuu	RW	7	aev	Mirror

register name : mirror								
register #	bit#	name	default	**U**	default(h)	**UU**	default(b)	**xxxxxxuu**
05d (05h)	7	x	0	Reserved				
	6	x	0	Reserved				
	5	x	0	Reserved				
	4	x	0	Reserved				
	3	x	0	Reserved				
	2	x	0	Reserved				
	1	vm	U	Vertical mirror ON/OFF				
	0	hm	U	Horizontal mirror ON/OFF				

▷ ***vm/hm***

default value : U wire-strapping register

The default value of this register is changed by wire-strapping. After changed wire-strapping, the register can be set with other values through SCL and SDA.

< Group A >

(6~11) FrameWidth, FrameHeight

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
6	06	framewidth_h	u	u	uuuuuuuu	RW	7	aev	Framewidth
7	07	framewidth_l	u	u	uuuuuuuu	RW	7	aev	
8	08	fd_fheight_a_h	2	02	xxx00010	RW	6	aev	Frameheight
9	09	fd_fheight_a_l	u	u	uuuuuuuu	RW	7	aev	
10	0A	fd_fheight_b_h	2	02	xxx00010	RW	6	aev	
11	0B	fd_fheight_b_l	u	u	uuuuuuuu	RW	7	aev	

▷ **FrameWidth, FrameHeight**

default value : U wire-strapping register

FrameWidth is the number of columns to be counted during one line time. FrameHeight is the number of rows. Column(Row) counter value is incremented 1 by 1 until it reaches FrameWidth(FrameHeight), then it is reset to 0. FrameHeight and FrameWidth determines the frame rate. Frame rate is given as follows.

Frame Rate = freq (pclk) / ((FrameHeight +1) X (FrameWidth+1))
Ex.) Pixel clock (pclk) = 13.5MHz, FrameWidth = 857d, FrameHeight = 524d, then the frame rate is 30 fps.

If user increase Frame Height at 2 times, Frame Rate is decreased by half.

▶ fd_fheight_a : flicker A state frameheight
▶ fd_fheight_b : flicker B state frameheight

< Group A >

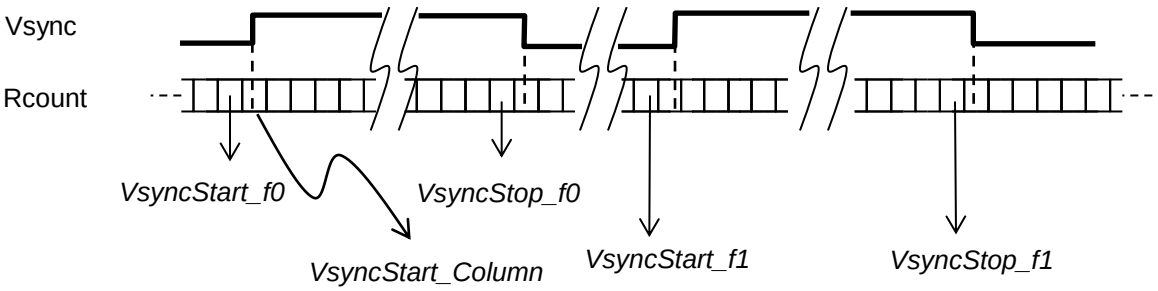
< Group A >

(20~29) Vsync Row Start/Stop, Vsync Column Start

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
20	14	vsyncstartrow_f0_h	0	00	xxx00000	RW	6	aev	Vsync generation
21	15	vsyncstartrow_f0_l	23	17	00010111	RW	6	aev	
22	16	vsyncstoprow_f0_h	1	01	xxx00001	RW	6	aev	
23	17	vsyncstoprow_f0_l	u	u	uuuuuuuu	RW	7	aev	
24	18	vsyncstartrow_f1_h	1	01	xxx00001	RW	6	aev	
25	19	vsyncstartrow_f1_l	u	u	uuuuuuuu	RW	7	aev	
26	1A	vsyncstoprow_f1_h	2	02	xxx00010	RW	6	aev	
27	1B	vsyncstoprow_f1_l	u	u	uuuuuuuu	RW	7	aev	
28	1C	vsynccolumn_h	0	00	xxxx0000	RW	5	0	
29	1D	vsynccolumn_l	2	02	00000010	RW	5	0	

▷ Output Vsync Generation

default value : U ➔ wire-strapping register



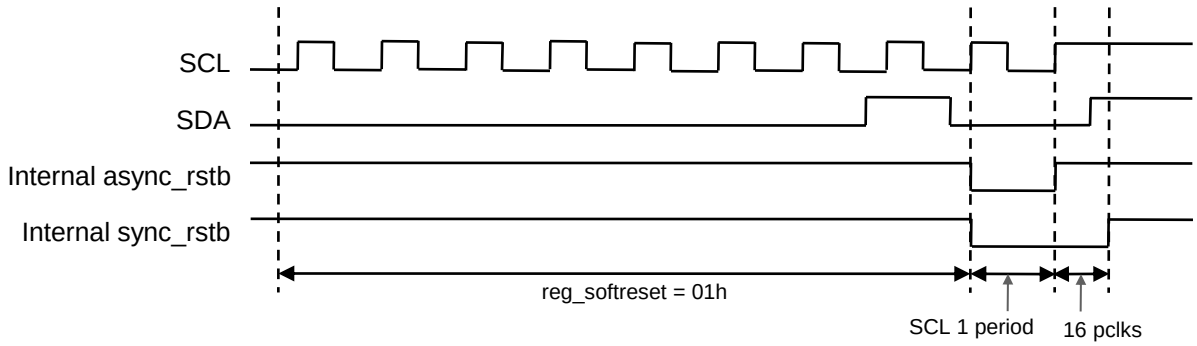
< Group A >

(36) Soft reset

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
36	24	softreset	0	00	xxxxxxx0	RW	5	0	Soft reset

▷ **Softreset**

PC7070K through I2C communication can be softreset.



(37) Clock divider

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
37	25	clkdiv	32	20	xx100000	RW	6	aev	Clock divider

▷ **Clock divider**

clkdiv[2:0]	ppclk
000b	mclk
001b	mclk * 2/3
010b	mclk * 1/2
011b	mclk * 1/3
100b	mclk * 1/4
101b	mclk * 1/8
else	mclk

clkdiv[4:3]	mclk
00b	vco
01b	vco * 1/2
10b	vco * 1/3
11b	vco * 1/4

clkdiv[5]	pclk
0b	ppclk/2
1b	ppclk

◆ **explain clocks.**
→ **pclk : The counter values increase at the pace of pclk.**
ppclk: essential clock for internal operation.
mclk: main clock.

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(39) Pad_control1

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
39	27	pad_control1	102	66	01100110	RW	5	0	Pad control

register name : pad_control1								
register #	bit#	name	default	**102**	default(h)	**66**	default(b)	**01100110**
39d (27h)	7	stdby	0	register stdby on/off ('1' : stdby mode, '0' : normal mode)				
	6	x	1	reserved				
	5	stdby_level	1	stdby data output pad level selector ("1x" : hiz, "01" : high, "00" : low)				
	4		0					
	3	clkoff	0	clock kill control register ('1' : clock Kill, '0' : not kill)				
	2	osc_pad_en	1	Osc(x1) pad enable				
	1	osc_pad_drv	1	Osc(x1) pad drivability				
	0		0					

(40) Pad_control2

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
40	28	pad_control2	0	00	00000000	RW	5	0	Pad control

register name : pad_control2								
register #	bit#	name	default	**0**	default(h)	**00**	default(b)	**00000000**
40d (28h)	7	pad_drv	0	Data & Vsync pad drivability control register				
	6		0					
	5	pclk_drv	0	PCLK drivability control				
	4		0					
	3	pclk_delay	0	PCLK delay control				
	2		0					
	1		0					
	0	pclk_pad_en	0	PCLK pad enable				

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(41) Pad_control3

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
41	29	pad_control3	0	00	00000000	RW	5	0	Pad control

register name : pad_control3								
register #	bit#	name	default	**0**	default(h)	**00**	default(b)	**00000000**
41d (29h)	7	vsync_pad_en	0	Vsync pad 0b : disable ,1b : enable				
	6	hsync_drv	0	Hsync drivability control				
	5		0					
	4	hsync_pad_en	0	Hsync pad 0b : disable ,1b : enable				
	3	d1_pad_en	0	Data1 pad 0b : disable ,1b : enable				
	2	d0_pad_en	0	Data0 pad 0b : disable, 1b : enable				
	1	x	0	Reserved				
	0	d_pad_selection	0	Data pad selection bit 0b : ISP data, 1b : manual(pad_control9)				

(42) Pad_control4

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
42	2A	pad_control4	0	00	00000000	RW	5	0	Pad control

register name : pad_control4								
register #	bit#	name	default	**0**	default(h)	**00**	default(b)	**00000000**
42d (2Ah)	7	ledctrl_en	0	LED pad 0b : disable ,1b : enable				
	6	ledctrl_pad_drv	0	LED pad drivability control				
	5		0					
	4	x	0	Reserved				
	3	x	0	Reserved				
	2		0					
	1		0					
	0		0					

< Group A >

(43) Pad_control5

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
43	2B	pad_control5	192	C0	11000000	RW	5	0	Pad control

register name : pad_control5								
register #	bit#	name	default	**192**	default(h)	**C0**	default(b)	**11000000**
43d (2Bh)	7	x	1	reserved				
	6	x	1	reserved				
	5	x	0	reserved				
	4	x	0	reserved				
	3	x	0	reserved				
	2	x	0	reserved				
	1	x	0	reserved				
	0	x	0	reserved				

(44) Pad_control6

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
44	2C	pad_control6	0	00	00000000	RW	5	0	Pad control

register name : pad_control6								
register #	bit#	name	default	**0**	default(h)	**00**	default(b)	**00000000**
44d (2Ch)	7	x	0	reserved				
	6	x	0	reserved				
	5	x	0	reserved				
	4	x	0	reserved				
	3	x	0	reserved				
	2	x	0	reserved				
	1	x	0	reserved				
	0	x	0	reserved				

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(45) Pad_control7

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
45	2D	pad_control7	0	00	00000000	RW	5	0	Pad control

register name : pad_control7								
register #	bit#	name	default	**0**	default(h)	**00**	default(b)	**00000000**
45d (2Dh)	7	x	0	Reserved				
	6	x	0	Reserved				
	5	x	0	Reserved				
	4	x	0	Reserved				
	3	x	0	Reserved				
	2	x	0	Reserved				
	1	x	0	Reserved				
	0	strap_smp	0	latch stores strap information when strap_smp='0'				

▷ ***Strap sampling***

For store the strap information .

When Vsync_pad_en or hsync_pad_en or data_pad_en or d0_pad_en is set as '1' strap_smp should be set as '1'.

Case of Master mode='1', strap_smp is automatically set as '1'.

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(46) Pad_control8

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
46	2E	pad_control8	0	00	00000000	RW	5	0	Pad control

register name : pad_control8								
register #	bit#	name	default	**0**	default(h)	**00**	default(b)	**00000000**
46d (2Eh)	7	d9_pad_en	0	d9 pad enable				
	6	d8_pad_en	0	d8 pad enable				
	5	d7_pad_en	0	d7 pad enable				
	4	d6_pad_en	0	d6 pad enable				
	3	d5_pad_en	0	d5 pad enable				
	2	d4_pad_en	0	d4 pad enable				
	1	d3_pad_en	0	d3 pad enable				
	0	d2_pad_en	0	d2 pad enable				

(47) Pad_control9

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
47	2F	pad_control9	0	00	00000000	RW	5	0	Pad control

register name : pad_control9								
register #	bit#	name	default	**0**	default(h)	**00**	default(b)	**00000000**
47d (2Fh)	7	d9_pad_manual	0	d9 pad manual output data				
	6	d8_pad_manual	0	d8 pad manual output data				
	5	d7_pad_manual	0	d7 pad manual output data				
	4	d6_pad_manual	0	d6 pad manual output data				
	3	d5_pad_manual	0	d5 pad manual output data				
	2	d4_pad_manual	0	d4 pad manual output data				
	1	d3_pad_manual	0	d3 pad manual output data				
	0	d2_pad_manual	0	d2 pad manual output data				

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(48) Strap_control

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
48	30	strap_control	255	FF	11111111	RW	5	0	Strap control

register name : strap_control								
register #	bit#	name	default	**255**	default(h)	**FF**	default(b)	**11111111**
48d (30h)	7	Strap master	1	I2C master strap control mode 1b : control when reset='0' ,0b : control in real-time				
	6	Strap General	1	General strap control mode 1b : control when reset='0' ,0b : control in real-time				
	5	OSD	1	OSD strap control mode 1b : control when reset='0' ,0b : control in real-time				
	4	Indoor / Outdoor	1	Indoor/Outdoor strap control mode 1b : control when reset='0' ,0b : control in real-time				
	3	BLC	1	BLC strap control mode 1b : control when reset='0' ,0b : control in real-time				
	2	Strap flicker	1	Flicker cancellation strap control mode 1b : control when reset='0' ,0b : control in real-time				
	1	Strap TV mode	1	TV mode strap control mode 1b : control when reset='0' ,0b : control in real-time				
	0	Strap Mirror	1	Horizontal & Vertical Mirror strap control mode 1b : control when reset='0' ,0b : control in real-time				

▷ ***Strap control***

***Strap_control*="FF"(default)**

:PC7070K strap information prior to the reset signal is applied.

***Strap_control*=" 00h"**

:The strap can be controlled in real time.

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(51) Pixelbias

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
51	33	pixelbias	8	08	xxxx1000	RW	5	0	Pixel bias

▷ **Pixelbias**

***Ipixel = *PixelBias* * (1/3)uA**

*** Pixel Bias range I= 0.35~5.5uA (bias control =0)**
0.25~3.8uA (bias control=1)

(52) compbias

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
52	34	compbias	5	05	xxx00101	RW	5	0	Comparator bias

▷ **Compbias**

I=2.84~46.86uA (1.42uA step)

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(79) Flicker control 1

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
79	4F	flicker_control1	u	u	uuuuuuuu	RW	5	0	Flicker control

register name : flicker_control1								
register #	bit#	name	default	**0**	default(h)	**00**	default(b)	**00000000**
79d (4Fh)	7	x	1	reserved				
	6	fd_en	0	flicker enable				
	5	x	0	reserved				
	4	x	0	reserved				
	3	manual_A	0	manual_A				
	2	manual_B	0	manual_B				
	1	x	0	reserved				
	0		0					

▷ ***fd_en***

default value : U wire-strapping register

Flicker detection enable/disable. .

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(89~94) Flicker control

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
89	59	fd_period_a_h	u	u	uuuuuuuu	RW	5	0	Flicker period for A state
90	5A	fd_period_a_m	u	u	uuuuuuuu	RW	5	0	
91	5B	fd_period_a_l	u	u	uuuuuuuu	RW	5	0	
92	5C	fd_period_b_h	1	01	00000001	RW	5	0	Flicker period for B state
93	5D	fd_period_b_m	u	u	uuuuuuuu	RW	5	0	
94	5E	fd_period_b_l	u	u	uuuuuuuu	RW	5	0	

▷ ***Flicker period A & B***

default value : U ➔ wire-strapping register

$$fd\_period\_a = \frac{256\ d^* \text{ pclk FREQ.}}{120d * framewidth}$$

$$fd\_period\_b = \frac{256\ d^* \text{ pclk FREQ.}}{100d * framewidth}$$

pclk FREQ.: frequency of pixel clock

< Group A >

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(123) LED control

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
123	7B	led_control1	1	01	00000001	RW	5	0	Auto Led control

register name : led_control1								
register #	bit#	name	default	**00**	default(h)	**00**	default(b)	**00000000**
123d (7Bh)	7	ledctrl en	0	Led control 0b : disable 1b : enable				
	6	x	0	reserved				
	5	ledctrl polarity	0	Led output polarity change 0b : disable 1b : enable				
	4	bwled en	0	Black & white mode @ led on 0b : disable 1b : enable				
	3	x	0	reserved				
	2	x	0	reserved				
	1	x	0	reserved				
	0	exrom_set_en	1	enable setting from external rom @ led on/off 0b: disable, 1b: enable				

▷ ***exrom_set enable***

led_control1[0]='1',according to LED on and LED off ,Initial code can be set different value when using external ROM(i2c)

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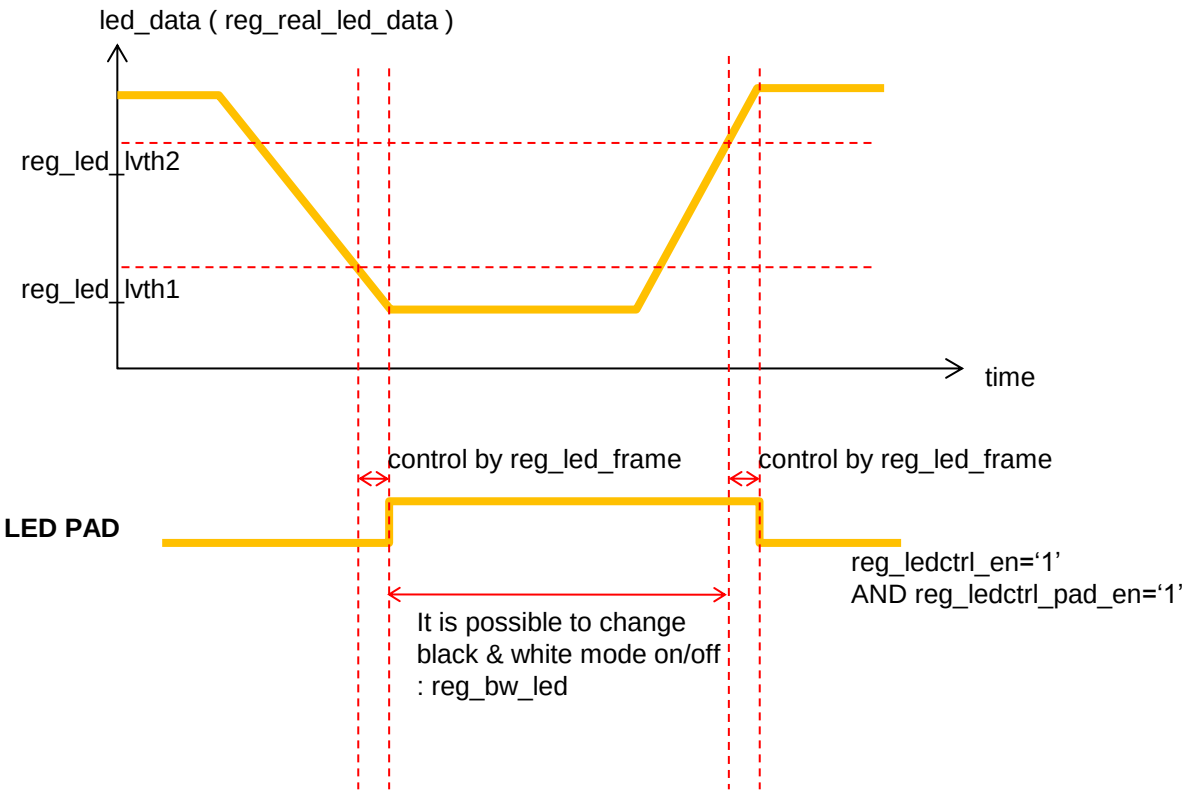
(124~126) LED control

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
124	7C	led_lvth1	0	00	00000000	RW	5	0	Led control level th.1
125	7D	led_lvth2	0	00	00000000	RW	5	0	Led control level th.2
126	7E	led_frame	128	80	10000000	RW	5	0	Led frame control



< Group A >

(162) spi osd control

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
162	A2	spi_osd_control	u	u	uuuuuuuu	RW	5	0	SPI OSD control

register name :spi_osd_control								
register #	bit#	name	default	**u**	default(h)	**uu**	default(b)	**uuuuuuuu**
162d (A2h)	7	x	0	Reserved				
	6	x	0	Reserved				
	5	x	0	Reserved				
	4	x	0	Reserved				
	3	x	0	Reserved				
	2	x	0	Reserved				
	1	x	0	Reserved				
	0	osd_enable	u	OSD display 0b: disable 1b: enable				

▷ ***OSD enable***

default value : U ➔ wire-strapping register

PC7070K is supported to 1layer OSD and It can be only used embedded PG.

If customer want to use Embedded PG, spi_osd_en and pg_enable should be set as '1'.

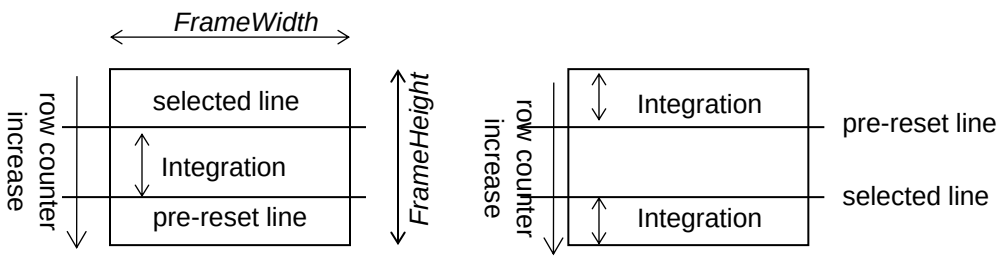
< Group B >

(444~446) Integration time.

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
444	BC	inttime_h	1	01	00000001	RW	6	aev	Integration time (line)
445	BD	inttime_m	64	40	01000000	RW	6	aev	
446	BE	inttime_l	0	00	00000000	RW	6	aev	Integration time (column)

▷ *integration time*

There are 3 bytes of registers to control the photo-charge accumulation interval for each pixel. DFh and E0h registers indicate how many line times the integration will continue until they are all reset. E1h register further sub-divides one line time into 256 smaller intervals. Total integration time is the sum of the integral multiple and fractional parts of one line time. As the row counter value is incremented from 0 to FrameHeight, each line relevant to the row count is selected and all pixel data of that line is read out all at once. The read- out operation involves pixel reset pulses, so all pixels that are selected and read out are reset to initial states. To control exposure time, there runs another counter to select and reset a line other than the one that is selected to be read out. The space between the two lines is equal to the number of integration lines. There are two possible situations concerning the position of selected line and reset line. The 1st case is where the pre-reset counter runs ahead of read-out counter. And the other case Is just the reverse of the 1st one. The number of integration lines is different for the two cases as is shown in the left figures. Since the basic unit of integration time for PC7070K is 1/ 256 line time, it is easy to implement Auto Exposure algorithms without worrying about strong light environment where the image may change abruptly in brightness or it may even blink.



Case 1. Reset line preceding select line Case 2. Select line preceding reset line

< Group B >

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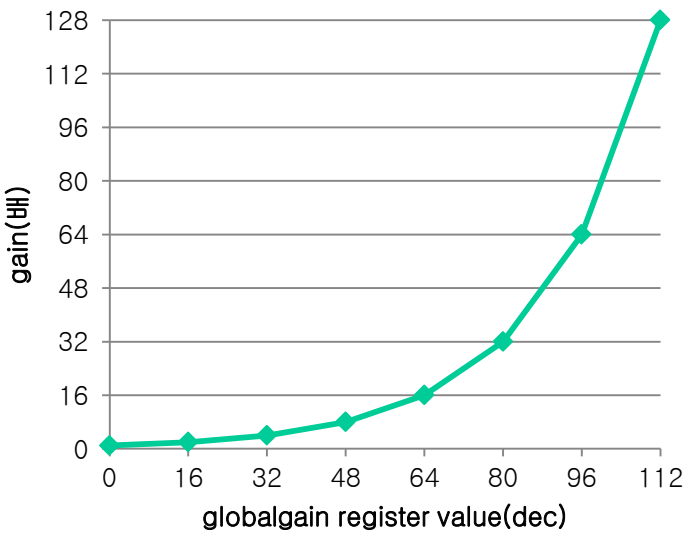
(447) Global gain

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
447	BF	globalgain	0	00	00000000	RW	6	aev	Analog gain

▷ *global gain*

GlobalGain has effect on all of R, G, and B pixel outputs. Raw R, G, B data are amplified by a common factor of GlobalGain.

The relation between GlobalGain and amplification factor is shown in the picture below.



(448) Digital gain

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
448	C0	digitalgain	64	40	01000000	RW	6	aev	Digital gain

▷ *digital gain*

digitalgain[7:6] : Integer
digitalgain[5:0] : Fraction

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(471) Real_led_data

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
471	D7	real_led_data	0	00	00000000	RO	0	0	Current CdS data

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▶ Register Tables (Detailed) : Group C

(516) ISP function control 0

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
516	04	isp_func_0	247	F7	11110111	RW	6	aev	Isp function control

register name : isp_func_0									
register #	bit#	name	default	**247**	default(h)	**F7**	default(b)	**11110111**	
516d (04h)	7	lens_en	1	Lens shading compensation 0b : disable, 1b : enable					
	6	x	1	reserved					
	5	x	1	reserved					
	4	x	1	reserved					
	3	x	0	reserved					
	2	x	1	reserved					
	1	ccr_en	1	Color correction 0b : disable, 1b : enable					
	0	x	1	reserved					

(517) ISP function control 1

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
517	05	isp_func_1	254	FE	11111110	RW	6	aev	Isp function control

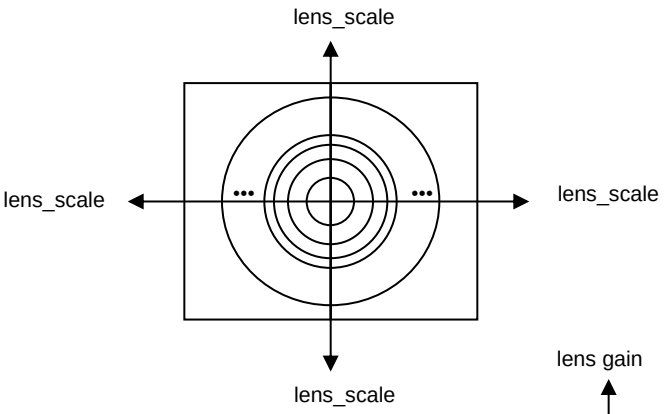
register name : isp_func_1									
register #	bit#	name	default	**254**	default(h)	**FE**	default(b)	**11111110**	
517d (05h)	7	x	1	reserved					
	6	x	1	reserved					
	5	x	1	reserved					
	4	x	1	reserved					
	3	edge_en	1	Edge enhancement 0b : disable, 1b : enable					
	2	x	1	reserved					
	1	x	1	reserved					
	0		0						

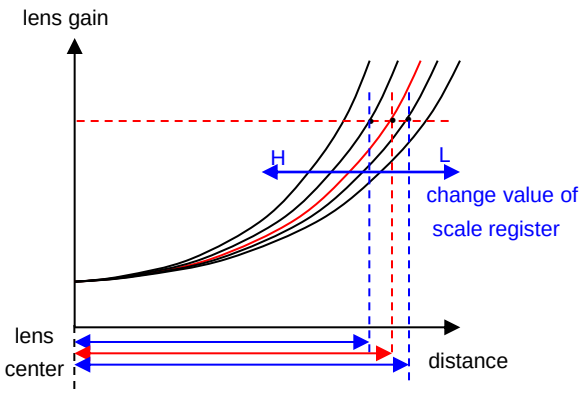
< Group C >

(526) Scale of lens shading compensation

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
526	0E	lens_scale	81	51	01010001	RW	5	0	Lens shading compensation scale control

▷ **lens scale**





< Group C >

(527~530) Lens gain

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
527	0F	lens_gainr	0	00	00000000	RW	6	aev	Lens shading compensation R gain
528	10	lens_gaing1	2	02	00000010	RW	6	aev	Lens shading compensation G1 gain
529	11	lens_gaing2	2	02	00000010	RW	6	aev	Lens shading compensation G2 gain
530	12	lens_gainb	0	00	00000000	RW	6	aev	Lens shading compensation B gain

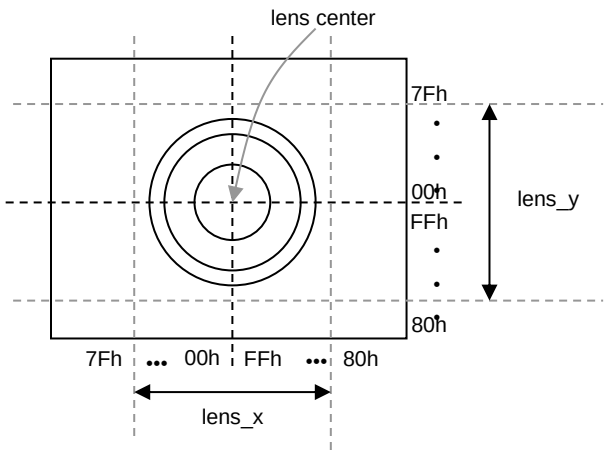
▷ **lens gain**

Lens Shading Gain : 0x20 = x 1 gain.

(531~532) Center control of lens shading compensation

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
531	13	lens_x	0	00	00000000	RW	5	0	Lens shading compensation center control
532	14	lens_y	0	00	00000000	RW	5	0	

▷ **lens shading center control**



< Group C >

< Group D >

(548~551) Edge gain control

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
548	24	edge_gain_ref0	32	20	00100000	RW	5	0	Edge gain fitting control
549	25	edge_gain_ref1	32	20	00100000	RW	5	0	
550	26	edge_gain_ref2	32	20	00100000	RW	5	0	
551	27	edge_gain	32	20	00100000	RW	6	aev	

▷ ***edge_gain_ref0/1/2***

Edge gain factor

★ ***edge_gain conditions :*** **00h ≤ edge_gain ≤ FFh**

< Group D >

< Group C >

(563~571) Color correction matrix

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
563	33	ccr_m11	43	2B	00101011	RW	5	0	Color correction matrix value
564	34	ccr_m12	138	8A	10001010	RW	5	0	
565	35	ccr_m13	129	81	10000001	RW	5	0	
566	36	ccr_m21	138	8A	10001010	RW	5	0	
567	37	ccr_m22	50	32	00110010	RW	5	0	
568	38	ccr_m23	136	88	10001000	RW	5	0	
569	39	ccr_m31	131	83	10000011	RW	5	0	
570	3A	ccr_m32	156	9C	10011100	RW	5	0	
571	3B	ccr_m33	63	3F	00111111	RW	5	0	

▷ color correction matrix

The color specifications of the image sensor differ from the fabrication process like color filter.

Due to the spectral characteristics of the optics, the native RGB data may not provide a faithful color rendition.

$$\begin{pmatrix} R' \\ G' \\ B' \end{pmatrix} = \begin{pmatrix} ccr\_m11 & ccr\_m12 & ccr\_m13 \\ ccr\_m21 & ccr\_m22 & ccr\_m23 \\ ccr\_m31 & ccr\_m32 & ccr\_m33 \end{pmatrix} \begin{pmatrix} R \\ G \\ B \end{pmatrix}$$

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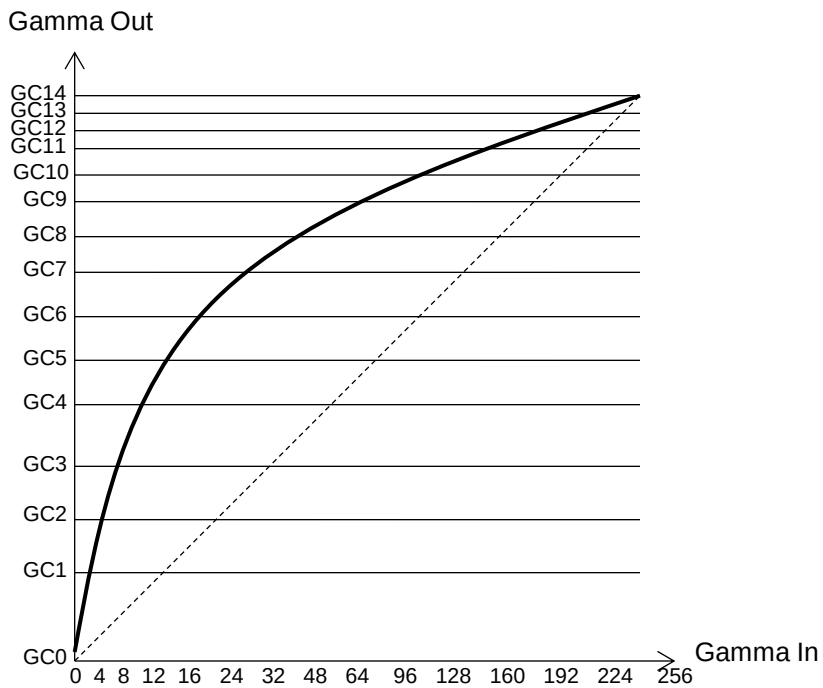
< Group C >

(573~587) Y Gamma1

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
573	3D	ygm1_y0	0	00	00000000	RW	5	0	Y gamma1 coefficient
574	3E	ygm1_y1	3	03	00000011	RW	5	0	
575	3F	ygm1_y2	12	0C	00001100	RW	5	0	
576	40	ygm1_y3	25	19	00011001	RW	5	0	
577	41	ygm1_y4	38	26	00100110	RW	5	0	
578	42	ygm1_y5	63	3F	00111111	RW	5	0	
579	43	ygm1_y6	82	52	01010010	RW	5	0	
580	44	ygm1_y7	110	6E	01101110	RW	5	0	
581	45	ygm1_y8	130	82	10000010	RW	5	0	
582	46	ygm1_y9	161	A1	10100001	RW	5	0	
583	47	ygm1_y10	185	B9	10111001	RW	5	0	
584	48	ygm1_y11	206	CE	11001110	RW	5	0	
585	49	ygm1_y12	224	E0	11100000	RW	5	0	
586	4A	ygm1_y13	240	F0	11110000	RW	5	0	
587	4B	ygm1_y14	255	FF	11111111	RW	5	0	

▷ *Y gamma1 coefficient*

Y Gamma1 Correction is applied to luminance signal which ranges from 0 to 255 to compensate non-linear characteristics of display brightness vs input brightness.



GC : Gamma coefficient

< Group C >

< Group C >

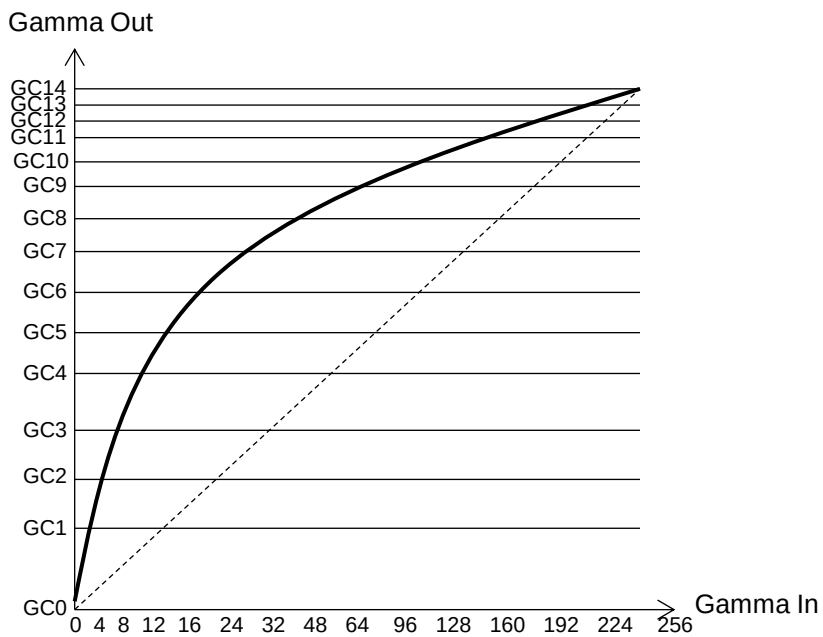
(588~602) Y Gamma2

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
588	4C	ygm2_y0	0	00	00000000	RW	5	0	Y gamma2 coefficient
589	4D	ygm2_y1	11	0B	00001011	RW	5	0	
590	4E	ygm2_y2	23	17	00010111	RW	5	0	
591	4F	ygm2_y3	34	22	00100010	RW	5	0	
592	50	ygm2_y4	46	2E	00101110	RW	5	0	
593	51	ygm2_y5	64	40	01000000	RW	5	0	
594	52	ygm2_y6	80	50	01010000	RW	5	0	
595	53	ygm2_y7	110	6E	01101110	RW	5	0	
596	54	ygm2_y8	136	88	10001000	RW	5	0	
597	55	ygm2_y9	174	AE	10101110	RW	5	0	
598	56	ygm2_y10	202	CA	11001010	RW	5	0	
599	57	ygm2_y11	220	DC	11011100	RW	5	0	
600	58	ygm2_y12	236	EC	11101100	RW	5	0	
601	59	ygm2_y13	246	F6	11110110	RW	5	0	
602	5A	ygm2_y14	255	FF	11111111	RW	5	0	

▷ *Y gamma2 coefficient*

Y Gamma2 Correction is applied to luminance signal which ranges from 0 to 255 to compensate non-linear characteristics of display brightness vs input brightness. In many cases, power function of 0.45 is used as gamma function for CRT display.

▶ Difference of Y Gamma1 and Y Gamma2 was selected by exposure.
When exposure's value is increasingly high, Y Output data is affected by the Y Gamma2.



GC : Gamma coefficient

< Group C >

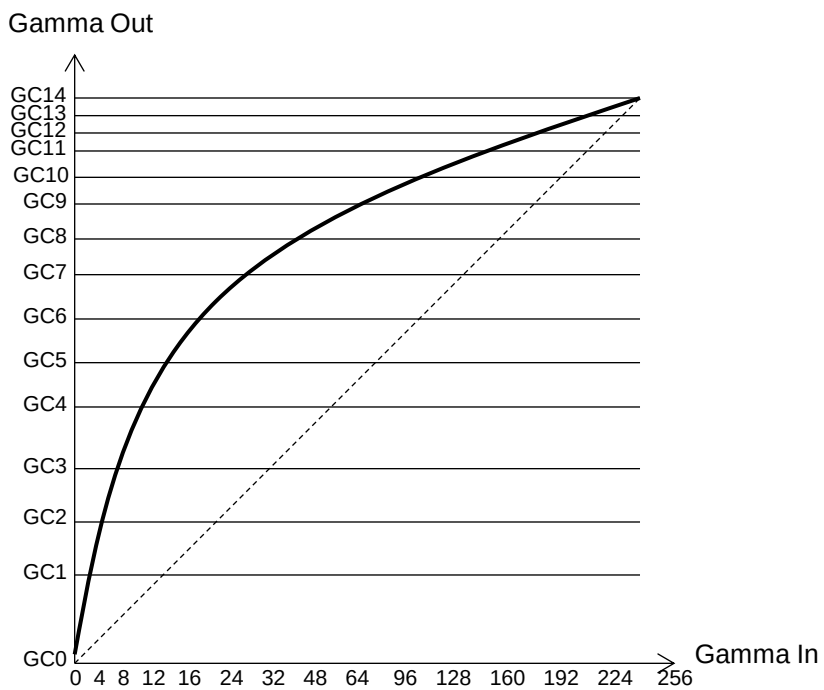
< Group C >

(603~617) RGB Gamma1

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
603	5B	cgm1_y0	0	00	00000000	RW	5	0	RGB gamma1 coefficient
604	5C	cgm1_y1	11	0B	00001011	RW	5	0	
605	5D	cgm1_y2	23	17	00010111	RW	5	0	
606	5E	cgm1_y3	34	22	00100010	RW	5	0	
607	5F	cgm1_y4	46	2E	00101110	RW	5	0	
608	60	cgm1_y5	64	40	01000000	RW	5	0	
609	61	cgm1_y6	80	50	01010000	RW	5	0	
610	62	cgm1_y7	110	6E	01101110	RW	5	0	
611	63	cgm1_y8	136	88	10001000	RW	5	0	
612	64	cgm1_y9	174	AE	10101110	RW	5	0	
613	65	cgm1_y10	202	CA	11001010	RW	5	0	
614	66	cgm1_y11	220	DC	11011100	RW	5	0	
615	67	cgm1_y12	236	EC	11101100	RW	5	0	
616	68	cgm1_y13	246	F6	11110110	RW	5	0	
617	69	cgm1_y14	255	FF	11111111	RW	5	0	

▷ RGB gamma1 coefficient

RGB Gamma1 Correction is applied to chrominance signal which ranges from 0 to 255 to compensate non-linear characteristics of display color vs input color.



GC : Gamma coefficient

< Group C >

< Group C >

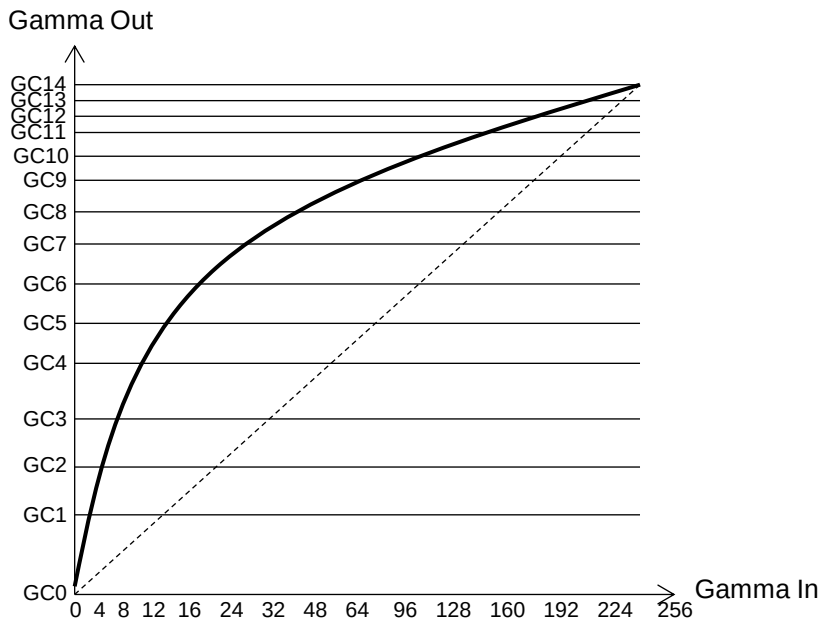
(618~632) RGB Gamma2

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
618	6A	cgm2_y0	0	00	00000000	RW	5	0	RGB gamma2 coefficient
619	6B	cgm2_y1	11	0B	00001011	RW	5	0	
620	6C	cgm2_y2	23	17	00010111	RW	5	0	
621	6D	cgm2_y3	34	22	00100010	RW	5	0	
622	6E	cgm2_y4	46	2E	00101110	RW	5	0	
623	6F	cgm2_y5	64	40	01000000	RW	5	0	
624	70	cgm2_y6	80	50	01010000	RW	5	0	
625	71	cgm2_y7	110	6E	01101110	RW	5	0	
626	72	cgm2_y8	136	88	10001000	RW	5	0	
627	73	cgm2_y9	174	AE	10101110	RW	5	0	
628	74	cgm2_y10	202	CA	11001010	RW	5	0	
629	75	cgm2_y11	220	DC	11011100	RW	5	0	
630	76	cgm2_y12	236	EC	11101100	RW	5	0	
631	77	cgm2_y13	246	F6	11110110	RW	5	0	
632	78	cgm2_y14	255	FF	11111111	RW	5	0	

▷ *RGB gamma2 coefficient*

RGB Gamma2 Correction is applied to chrominance signal which ranges from 0 to 255 to compensate non-linear characteristics of display color vs input color.

▶ Difference of RGB Gamma1 and RGB Gamma2 was selected by exposure. When exposure's value is increasingly high, RGB Output data is affected by the Y Gamma2.



GC : Gamma coefficient

< Group C >

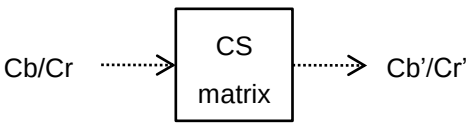
(640~643) Color saturation

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
640	80	cs11	37	25	00100101	RW	6	aev	Color saturation matrix value
641	81	cs12	0	00	00000000	RW	6	aev	
642	82	cs21	0	00	00000000	RW	6	aev	
643	83	cs22	37	25	00100101	RW	6	aev	

▷ ***CS11/12/21/22***

Color Saturation matrix control register

$$\begin{bmatrix} Cb' \\ Cr' \end{bmatrix} = \begin{bmatrix} Cs11 & Cs12 \\ Cs21 & Cs22 \end{bmatrix} \begin{bmatrix} Cb \\ Cr \end{bmatrix}$$



(660~664) Ycontrast and ybrightness

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
660	94	ycontrast	64	40	01000000	RW	6	aev	Y contrast
661	95	ybrightness_ref0	0	00	00000000	RW	5	0	Y brightness fitting control
662	96	ybrightness_ref1	0	00	00000000	RW	5	0	
663	97	ybrightness_ref2	0	00	00000000	RW	5	0	
664	98	ybrightness	0	00	00000000	RW	6	aev	

▷ ***Y contrast***

▶ **ycontrast *conditions :* 00h ≤ ycontrast ≤ FFh**

▷ ***Y brightness***

Y brightness registers.(2's complement)

filter_control1[5]* = '0b' : manually *ybrightness.

***filter_control1[5]* = '1b' : Automatically *ybrightness*.**

ycontrast_ref0 ~ 2 (E_8Eh ~ 96h) register by the y-axis reference point three sets.

★ ***ybrightness conditions* are given as**

-128d ≤ ybrightness ≤ 127d

< Group C >

< Group C >

(667) Sync control 1

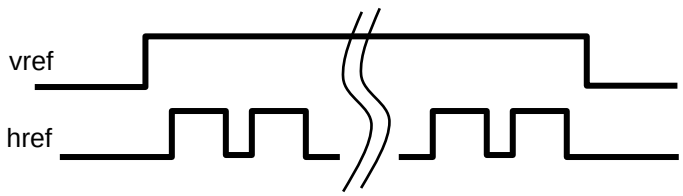
address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
667	9B	sync_control_1	0	00	00000000	RW	6	aev	Sync control

register name : sync_control_1								
register #	bit#	name	default	**0**	default(h)	**00**	default(b)	**00000000**
667d (9Bh)	7	x	0	reserved				
	6	sync_vsyncPolarity	0	vsync polarity change				
	5	sync_hsyncAllLines	0	hsync output all lines enable(black and active)				
	4	sync_hsyncPolarity	0	hsync polarity change				
	3	sync_pclkwindow	0	pclk window				
	2	sync_pclkPolarity	0	pclk polarity change				
	1	x	0	reserved				
	0	x	0	reserved				

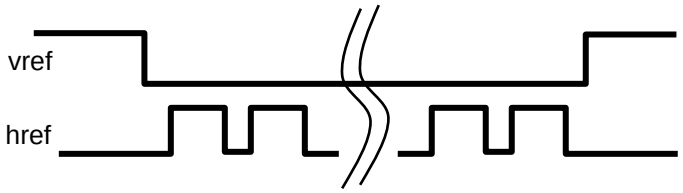
▷ ***Sync_vsyncpolarity***

Vsync output polarity control register.

▶ vsyncPolarity = '0'



▶ vsyncPolarity = '1'

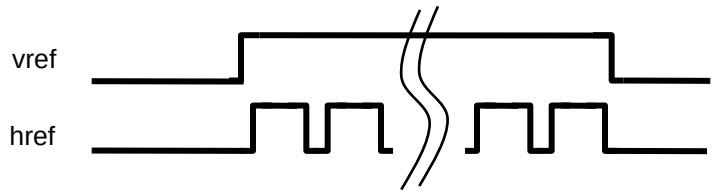


< Group C >

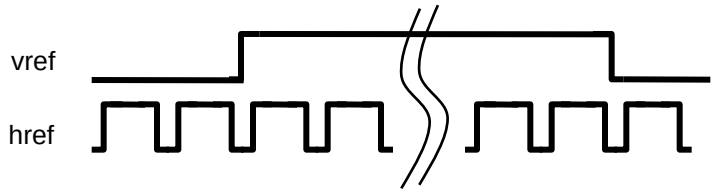
▷ *Sync_hsyncAllLines*

Hsync output control register

▶ hsyncAllLines = '0'



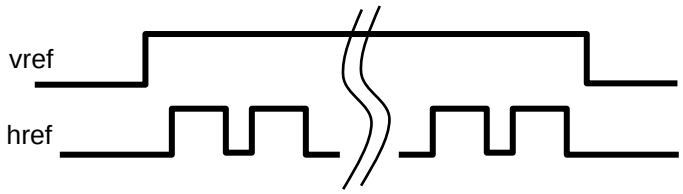
▶ hsyncAllLines = '1'



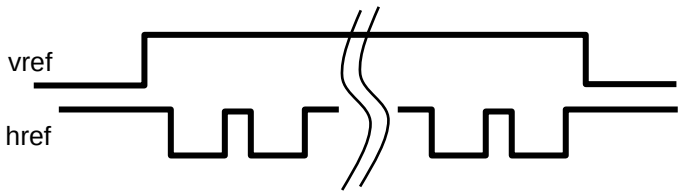
▷ *Sync_hsyncpolarity*

Hsync output polarity control register.

▶ hsyncPolarity = '0'



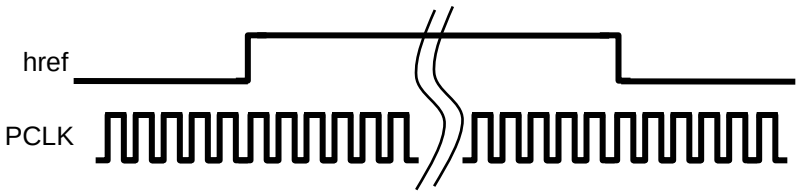
▶ hsyncPolarity = '1'



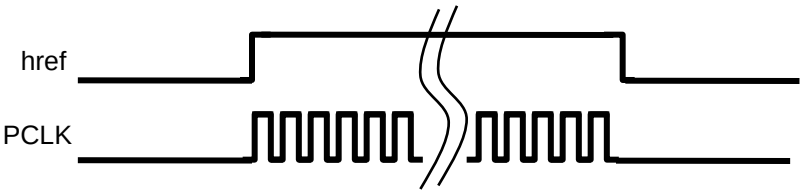
▷ Sync_pclkwindow

Pclk output control register

▶ pclkwindow = '0'



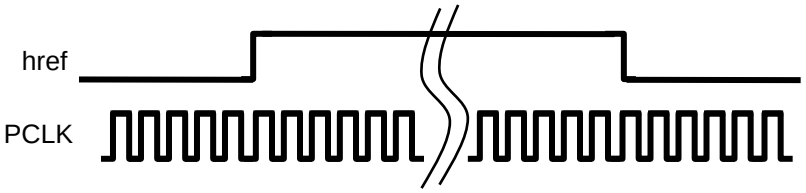
▶ pclkwindow = '1'



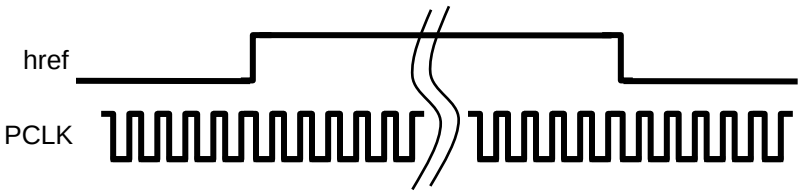
▷ *Sync_pclkpolarity*

Pclk output polarity control register

▶ pclkpolarity = '0'



▶ pclkpolarity = '1'



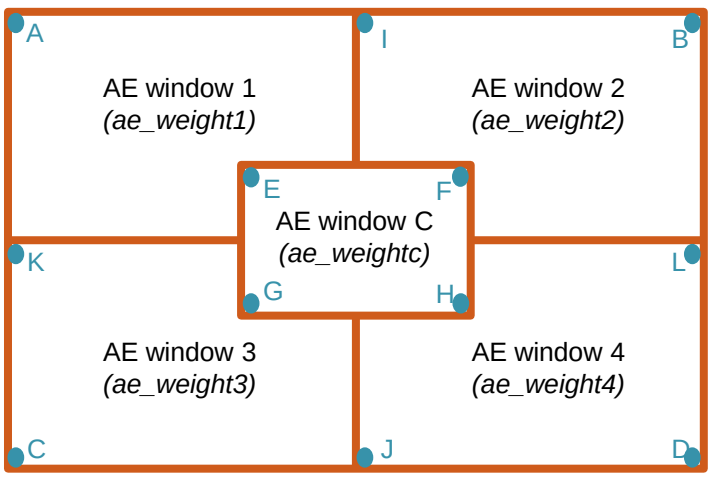
< Group C >

(691~710) Auto exposure window control

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
691	B3	ae_fwx1_h	0	00	xxxxxx00	RW	5	0	AE full window X start position
692	B4	ae_fwx1_l	1	01	00000001	RW	5	0	
693	B5	ae_fwx2_h	2	02	xxxxxx10	RW	5	0	AE full window X stop position
694	B6	ae_fwx2_l	128	80	10000000	RW	5	0	
695	B7	ae_fwy1_h	0	00	xxxxxx00	RW	5	0	AE full window Y start position
696	B8	ae_fwy1_l	1	01	00000001	RW	5	0	
697	B9	ae_fwy2_h	1	01	xxxxxx01	RW	5	0	AE full window Y stop position
698	BA	ae_fwy2_l	224	E0	11100000	RW	5	0	
699	BB	ae_cwx1_h	0	00	xxxxxx00	RW	5	0	AE center window X start position
700	BC	ae_cwx1_l	214	D6	11010110	RW	5	0	
701	BD	ae_cwx2_h	1	01	xxxxxx01	RW	5	0	AE center window X stop position
702	BE	ae_cwx2_l	171	AB	10101011	RW	5	0	
703	BF	ae_cwy1_h	0	00	xxxxxx00	RW	5	0	AE center window Y start position
704	C0	ae_cwy1_l	161	A1	10100001	RW	5	0	
705	C1	ae_cwy2_h	1	01	xxxxxx01	RW	5	0	AE center window Y stop position
706	C2	ae_cwy2_l	64	40	01000000	RW	5	0	
707	C3	ae_xaxis_h	1	01	xxxxxx01	RW	5	0	AE window X axis
708	C4	ae_xaxis_l	65	41	01000001	RW	5	0	
709	C5	ae_yaxis_h	0	00	xxxxxx00	RW	5	0	AE window Y axis
710	C6	ae_yaxis_l	241	F1	11110001	RW	5	0	

▷ AE window control

AE window control registers



A : *(ae_fwx1, ae_fwy1)*
B : *(ae_fwx2, ae_fwy1)*
C : *(ae_fwx1, ae_fwy2)*
D : *(ae_fwx2, ae_fwy2)*
E : *(ae_cwx1, ae_cwy1)*
F : *(ae_cwx2, ae_cwy1)*
G : *(ae_cwx1, ae_cwy2)*
H : *(ae_cwx2, ae_cwy2)*
I : *(ae_xaxis, ae_fwy1)*
J : *(ae_xaxis, ae_fwy2)*
K : *(ae_fwx1, ae_yaxis)*
L : *(ae_fwx2, ae_yaxis)*

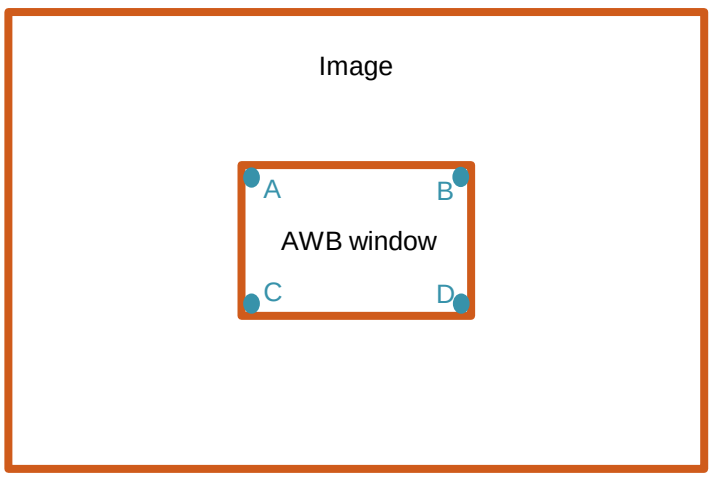
< Group C >

(711~718) AWB window control

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
711	C7	awb_wx1_h	0	00	xxxxxx00	RW	5	0	AWB window X start position
712	C8	awb_wx1_l	1	01	00000001	RW	5	0	
713	C9	awb_wx2_h	2	02	xxxxxx10	RW	5	0	AWB window X stop position
714	CA	awb_wx2_l	128	80	10000000	RW	5	0	
715	CB	awb_wy1_h	0	00	xxxxxx00	RW	5	0	AWB window Y start position
716	CC	awb_wy1_l	1	01	00000001	RW	5	0	
717	CD	awb_wy2_h	1	01	xxxxxx01	RW	5	0	AWB window Y stop position
718	CE	awb_wy2_l	224	E0	11100000	RW	5	0	

▷ *AWB window control*

AWB window control registers.



A : *(awb_wx1, awb_wy1)*
B : *(awb_wx2, awb_wy1)*
C : *(awb_wx1, awb_wy2)*
D : *(awb_wx2, awb_wy2)*

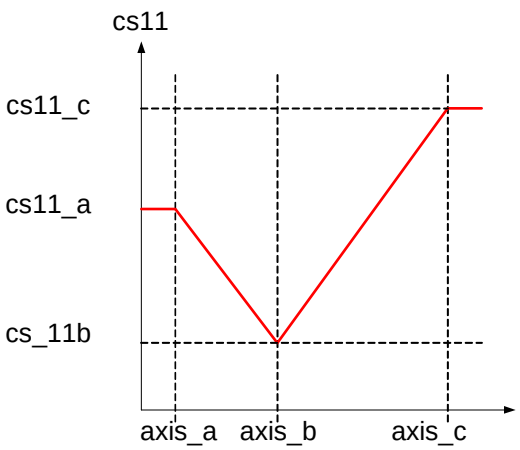
▶ Register Tables (Detailed) : Group D

< Group D >

(772~787) CS matrix fitting reference

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
772	04	cs11_a	40	28	00101000	RW	5	0	Color saturation matrix fitting reference
773	05	cs12_a	0	00	00000000	RW	5	0	
774	06	cs21_a	0	00	00000000	RW	5	0	
775	07	cs22_a	40	28	00101000	RW	5	0	
776	08	cs11_b	36	24	00100100	RW	5	0	
777	09	cs12_b	0	00	00000000	RW	5	0	
778	0A	cs21_b	0	00	00000000	RW	5	0	
779	0B	cs22_b	40	28	00101000	RW	5	0	
780	0C	cs11_c	32	20	00100000	RW	5	0	
781	0D	cs12_c	0	00	00000000	RW	5	0	
782	0E	cs21_c	0	00	00000000	RW	5	0	
783	0F	cs22_c	32	20	00100000	RW	5	0	
784	10	axis_a	58	3A	00111010	RW	5	0	CS matrix / lens gain fitting reference
785	11	axis_b	84	54	01010100	RW	5	0	
786	12	axis_c	89	59	01011001	RW	5	0	
787	13	user_cs	56	38	00111000	RW	5	0	User CS gain

▷ CS matrix fitting reference



*** Calculation method of cs12, cs21 and cs22 are same as calculation method of cs11.**

*** bit define of cs11_a/b/c**
[7] : sign
[6:5] : magnitude of integer
[4:0] : magnitude of fraction

axis_a < axis_b < axis_c

< Group D >

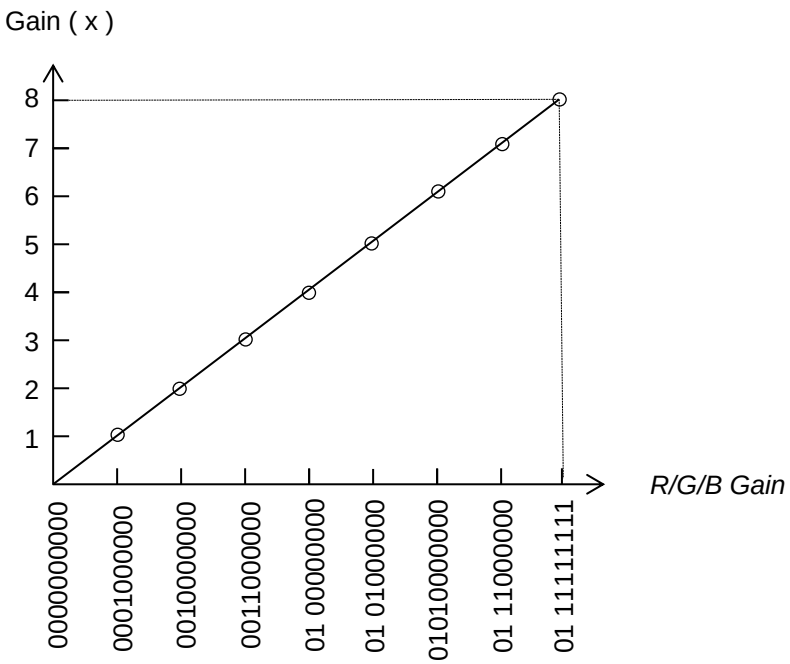
< Group D >

(795~800) Normalized white balance gain

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
795	1B	wb_rgain_h	0	00	00000000	RW	6	aev	Normalized white balance gain
796	1C	wb_rgain_l	93	5D	01011101	RW	6	aev	
797	1D	wb_ggain_h	0	00	00000000	RW	6	aev	
798	1E	wb_ggain_l	64	40	01000000	RW	6	aev	
799	1F	wb_bgain_h	0	00	00000000	RW	6	aev	
800	20	wb_bgain_l	94	5E	01011110	RW	6	aev	

▷ *wb_r/g/bgain*

When operating awb_normalization function, If one of wb_gain is lower than 40h, that is replace 40h, and other wb gain is calculated that other wb gain is multiply same weight.



gain_h[1:0] : integer

gain_l[7:6] : Integer

gain_l[5:0] : Fraction

(854~857) dark CCR for color correction

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
854	56	dark_ccr0	0	00	00000000	RW	5	0	Dark color correction fitting control
855	57	dark_ccr1	128	80	10000000	RW	5	0	
856	58	dark_ccr2	255	FF	11111111	RW	5	0	
857	59	dark_ccr	0	00	00000000	RW	6	aev	

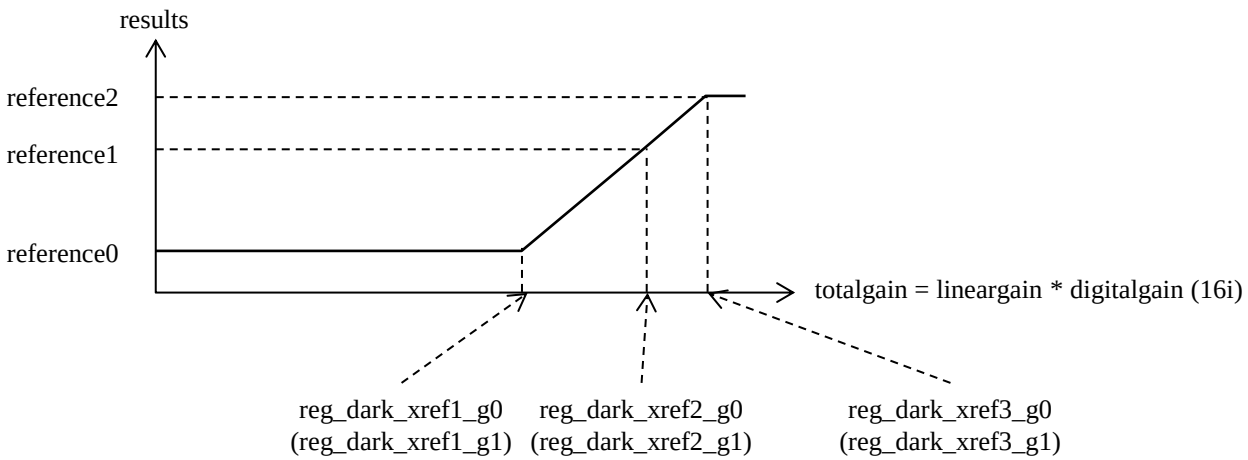
▷ ***dark_ccr***

Color correction control registers.

When dark_ccr is set to bigger value, color correction is weakness.

***filter_control1[7]* = '1b' : dark_ccr is fitting as below graph.**
***filter_control1[7]* = '0b' : user can program dark_ccr manually.**

★ ***dark_ccr conditions :* 00h ≤ dark_ccr0 ≤ dark_ccr1, dark_ccr2 ≤ FFh**
dark_ccr0 ≤ 0Fh



< Group D >

(869~876) ec_pth / ec_mth dark filter

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
869	65	dark_ec_pth0	4	04	00000100	RW	5	0	Dark edge clamp plus threshold filter control
870	66	dark_ec_pth1	80	50	01010000	RW	5	0	
871	67	dark_ec_pth2	160	A0	10100000	RW	5	0	
872	68	dark_ec_pth	4	04	00000100	RW	6	aev	
873	69	dark_ec_mth0	4	04	00000100	RW	5	0	Dark edge clamp minus threshold filter control
874	6A	dark_ec_mth1	64	40	01000000	RW	5	0	
875	6B	dark_ec_mth2	128	80	10000000	RW	5	0	
876	6C	dark_ec_mth	4	04	00000100	RW	6	aev	

▷ *ec_pth / ec_mth dark filter*

edge clamp threshold registers.

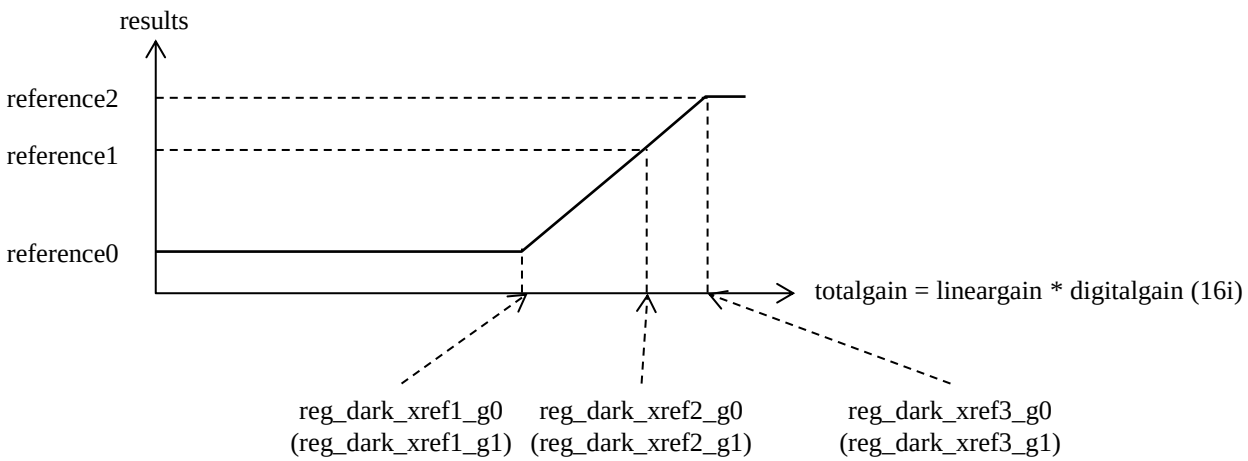
When dark_ec_pth is set to bigger value , positive edge part is darkness.
When dark_ec_mth is set to bigger value , negative edge part is brightness.

***filter_control1[7]* = '1b' : dark_ec_mth/pth is fitting as below graph.**
***filter_control1[7]* = '0b' : user can program dark_ec_mth/pth manually.**

★ ***dark_ec_pth / dark_ec_mth conditions* are given as**

00h ≤ dark_ec_pth ≤ FFh

00h ≤ dark_ec_mth ≤ FFh



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(887~890) de-color dark filter

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
887	77	dark_dc0	0	00	00000000	RW	5	0	de-color dark filter fitting control
888	78	dark_dc1	0	00	00000000	RW	5	0	
889	79	dark_dc2	6	06	00000110	RW	5	0	
890	7A	dark_dc	0	00	00000000	RW	6	aev	

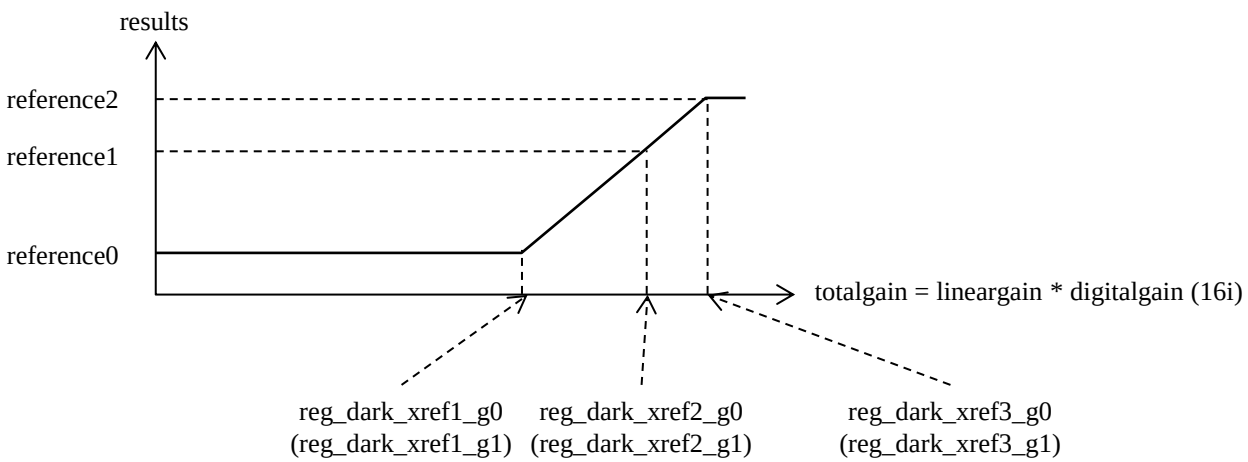
▷ de-color dark filter

De-color registers.

When dark_dc is set to bigger value , color supress is more effective.

***filter_control1[7]* = '1b' : dark_dc is fitting as below graph.**
***filter_control1[7]* = '0b' : user can program dark_dc manually.**

★ ***dark_dc conditions :* 00h ≤ dark_dc ≤ 3Fh**



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(919~926) y_cont_th2/y_cont_slope2

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
919	97	y_cont_th2_ref0	128	80	10000000	RW	5	0	Dark y contrast th2 fitting control
920	98	y_cont_th2_ref1	128	80	10000000	RW	5	0	
921	99	y_cont_th2_ref2	128	80	10000000	RW	5	0	
922	9A	y_cont_th2	128	80	10000000	RW	6	aev	
923	9B	y_cont_slope2_ref0	64	40	01000000	RW	5	0	Dark y contrast slope2 fitting control
924	9C	y_cont_slope2_ref1	64	40	01000000	RW	5	0	
925	9D	y_cont_slope2_ref2	64	40	01000000	RW	5	0	
926	9E	y_cont_slope2	64	40	01000000	RW	6	aev	

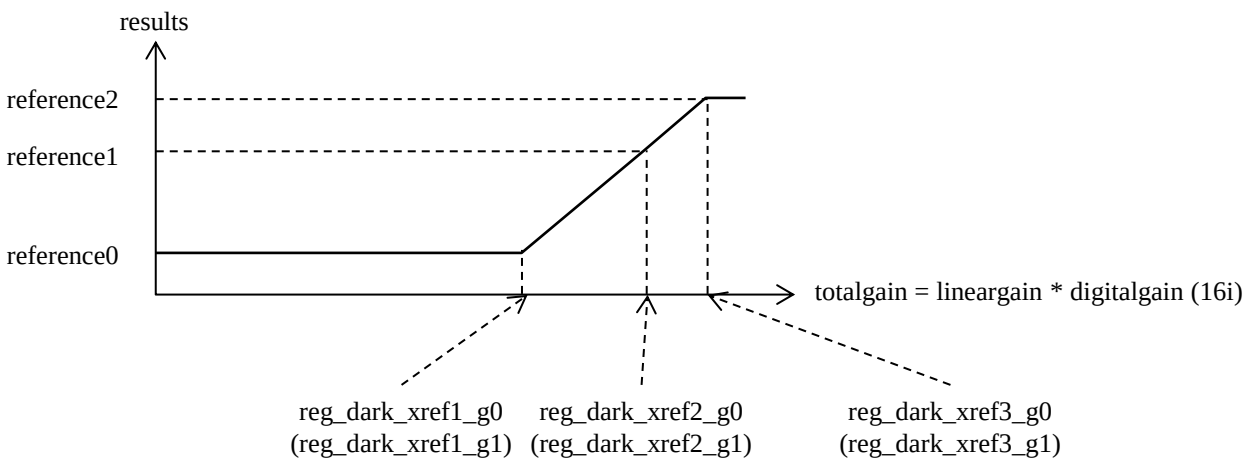
▷ y_cont_th2/y_cont_slope2

y contrast slope2/th2 control registers.

Fiducially y_cont_th2, brightness part is more brighter, darkness part is more darker.

***filter_control1[7]* = '1b' : y_cont_th2/y_cont_slope2 is fitting as below graph.**
***filter_control1[7]* = '0b' : user can program y_cont_th2/y_cont_slope2 manually.**

★ ***y_cont_th2/ y_cont_slope2 conditions :* 00h ≤ y_cont_th2/ y_cont_slope2 ≤ FFh**



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▶ Register Tables (Detailed) : Group E

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(1028) Auto_control_1

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1028	04	auto_control_1	152	98	10011000	RW	6	autov	Auto control

register name : auto_control_1								
register #	bit#	name	default	**152**	default(h)	**98**	default(b)	**10011000**
1028d (04h)	7	x	1	reserved				
	6	x	0	reserved				
	5	x	0	reserved				
	4	x	1	reserved				
	3	x	1	reserved				
	2	AWB mode	0	White blance mode selection 0b : auto mode, 1b : manual mode				
	1	exposure mode	0	Exposure mode selection 00b : auto mode 01b : manual mode (exposure write) 10b : manual mode (ext_inttime, ext_glbgain write) 11b : manual mode (inttime, globalgain write)				
	0		0					

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▷ AWB mode

When auto_control_1[2] is '1', auto white balance dose not operation and you can write. white balance gain(Reg. D-1Bh~20h). Please set disable, before writing white balance gain.

▷ AE mode

PC7070K provides auto exposure mode and 3 type of manual exposure mode.
User can select auto exposure mode by writing auto_control_1[1:0].

▶ auto_control_1[1:0] = 00b (auto exposure mode)
When auto_control_1[1:0] is 00h, integration time, global gain and digital gain are calculated by auto exposure block. Refer to auto exposure reference register(Reg. E-12h~20h).

▶ auto_control_1[1:0] = 01b (manual exposure mode1)
When auto_control_1[1:0] is 01h, integration time, global gain and digital by exposure register(Reg. E-27~2Ah).

▶ auto_control_1[1:0] = 10b (manual exposure mode2)
When auto_control_1[1:0] is 10h, you can control integration time, global gain and digital gain by external integration time and external linear global gain register(Reg. E-22h~26h).

▶ auto_control_1[1:0] = 11b (manual exposure mode3)
When auto_control_1[1:0] is 11h, you can write integration time, global gain register. Refer to Reg. B_BCh~C0h

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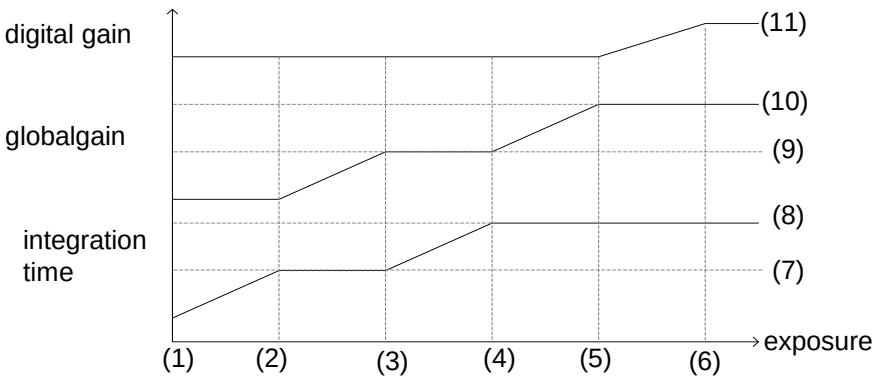
(1042~1056) AE reference registers

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1042	12	expfrmh_h	2	02	00000010	RW	5	0	AE reference
1043	13	expfrmh_l	u	u	uuuuuuuu	RW	5	0	
1044	14	midfrmheight_h	2	02	00000010	RW	5	0	
1045	15	midfrmheight_l	u	u	uuuuuuuu	RW	5	0	
1046	16	maxfrmheight_h	2	02	00000010	RW	5	0	
1047	17	maxfrmheight_l	u	u	uuuuuuuu	RW	5	0	
1048	18	minexp_h	0	00	00000000	RW	5	0	
1049	19	minexp_m	0	00	00000000	RW	5	0	
1050	1A	minexp_l	12	0C	00001100	RW	5	0	
1051	1B	midexp_t	1	01	00000001	RW	5	0	
1052	1C	midexp_h	129	81	10000001	RW	5	0	
1053	1D	midexp_m	128	80	10000000	RW	5	0	
1054	1E	maxexp_t	3	03	00000011	RW	5	0	
1055	1F	maxexp_h	3	03	00000011	RW	5	0	
1056	20	maxexp_m	0	00	00000000	RW	5	0	

▷ *AE reference registers*

default value : U wire-strapping register

When auto_control_1[1:0] is 00b or 01b, integration time, globalgain and digitalgain are calculated using AE reference registers.



(1) minimum exposure
(2) frame height for exposure
(3) mid frame height for exposure
(4) max frame height for exposure
(5) mid exposure
(6) max exposure
(7) mid integration time = (2)
(8) max integration time = (4)/(9)
(9) mid globalgain = (3)/(2)
(10) max globalgain =(5)/(8)
(11) max digital gain = (6)/{ (10)*(8) }

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(1058~1062) Manual integration time and linear globalgain for external AE mode

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1058	22	ext_inttime_h	0	00	00000000	RW	6	autov	Manual integration time @ external AE mode
1059	23	ext_inttime_m	128	80	10000000	RW	6	autov	
1060	24	ext_inttime_l	0	00	00000000	RW	6	autov	
1061	25	ext_glbg_h	1	01	00000001	RW	6	autov	Manual analog gain @ external AE mode
1062	26	ext_glbg_l	0	00	00000000	RW	6	autov	

▷ *ext_inttime*

When auto_control_1[1:0] is 10b, user can control integration time by writing external integration time registers.

Ext_inttime_h and ext_inttime_m are line of external integration time.

Ext_inttime_l is column of external integration time.

Prior to write External integration time, should be set as *auto_control_1[1:0]* = "10b".

▷ *ext_globalgain*

When auto_control_1[1:0] is 10b, user can control globalgain by writing external linear globalgain registers.

Globalgain is calculated by external linear globalgain and reference gain in manual exposure mode 2.

Set auto_control_1[1:0] to 10b, before writing external integration time.

(1063~1066) Exposure

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1063	27	exposure_t	0	00	00000000	RW	6	autov	Exposure
1064	28	exposure_h	1	01	00000001	RW	6	autov	
1065	29	exposure_m	64	40	01000000	RW	6	autov	
1066	2A	exposure_l	0	00	00000000	RW	6	autov	

▷ *exposure*

When auto_control_1[1:0] is 00b, exposure registers are calculated by auto exposure block. Exposure registers are used in calculating integration time, globalgain and digital gain.

When auto_control_1[1:0] is 01b, user can write exposure registers.

Set auto_control_1[1:0] to 01b, before writing exposure registers.

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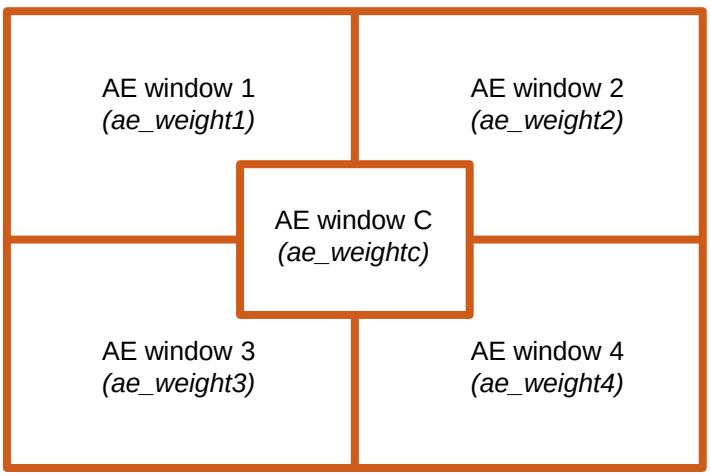
(1072~1076) AE weight

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1072	30	ae_weight1	8	08	xx001000	RW	5	0	AE weight peripheral
1073	31	ae_weight2	8	08	xx001000	RW	5	0	
1074	32	ae_weight3	8	08	xx001000	RW	5	0	
1075	33	ae_weight4	8	08	xx001000	RW	5	0	
1076	34	ae_weightc	8	08	xx001000	RW	5	0	AE weight center

▷ **ae_weight1/2/3/4/c**

AE data weight for BLC(back light compensation)



(1081~1082) Y mean reference & Y mean

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1081	39	ymean_h	0	00	00000000	RW	5	0	Y mean
1082	3A	ymean_l	128	80	10000000	RW	5	0	

(1083~1086) Min/Max Y target reference

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1083	3B	max_yt1	160	A0	10100000	RW	6	autov	Min / max ytarget control reference
1084	3C	max_yt2	128	80	10000000	RW	6	autov	
1085	3D	min_yt1	120	78	01111000	RW	6	autov	
1086	3E	min_yt2	120	78	01111000	RW	6	autov	

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(1096~1097) AE speed

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1096	48	ae_up_speed	8	08	00001000	RW	6	autov	AE upside speed
1097	49	ae_down_speed	8	08	00001000	RW	6	autov	AE downside speed

▷ ***ae_up_speed & ae_down_speed***

yt ≥ ym : AE_speed = *ae_up_speed*
yt < ym : AE_speed = *ae_down_speed*

If ae_up_speed and ae_down_speed have high value, auto exposure speed will be faster. However, high ae_up_speed and ae_down_speed value may cause AE oscillation.

(1098) AE lock range

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1098	4A	ae_lock	16	10	00010000	RW	6	autov	AE lock range

▷ ***ae_lock***

AE lock range control register.

Setting range of ae_lock is 00h to FFh.
If ae_lock has low value, auto exposure lock range will be smaller.
However, small value of ae_lock may cause AE oscillation

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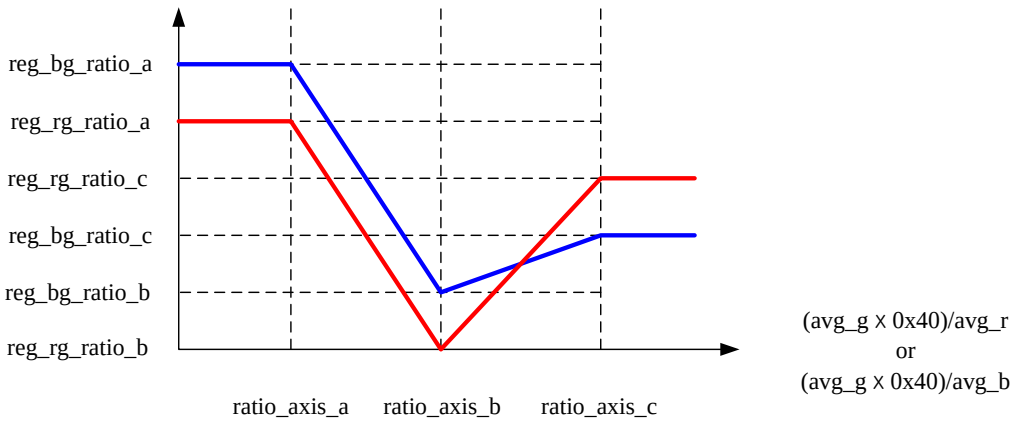
(1128~1138) rg/bg ratio reference & rg/bg ratio

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1128	68	rg_ratio_a	128	80	10000000	RW	5	0	Target awb ratio fitting reference
1129	69	bg_ratio_a	128	80	10000000	RW	5	0	
1130	6A	rg_ratio_b	128	80	10000000	RW	5	0	
1131	6B	bg_ratio_b	128	80	10000000	RW	5	0	
1132	6C	rg_ratio_c	128	80	10000000	RW	5	0	
1133	6D	bg_ratio_c	128	80	10000000	RW	5	0	
1134	6E	ratio_axis_a	58	3A	00111010	RW	5	0	
1135	6F	ratio_axis_b	84	54	01010100	RW	5	0	
1136	70	ratio_axis_c	89	59	01011001	RW	5	0	
1137	71	awb_rgratio	128	80	10000000	RW	5	0	AWB RG ratio control
1138	72	awb_bgratio	128	80	10000000	RW	5	0	AWB BG ratio control

▷ RG/BG_ratio_a/b/c

Target AWB ratio fitting reference

: These registers are used for deciding AWB target. It's possible to enable or disable these registers by controlling auto_control_3[7].



User can change the value of X-axis by using auto_cotnrol_3[6].

'1b': avg_gx0x40/avg_r
'0b': avg_gx0x40/avg_b

Caution) ratio_axis_a < ratio_axis_b < ratio_axis_c

▷ AWB_RG/BGratio

AWB target control registers

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(1139~1140) AWB lock range & speed

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1139	73	awb_lock	16	10	00010000	RW	5	0	AWB lock range
1140	74	awb_speed	4	04	00000100	RW	5	0	AWB speed

▷ ***AWB_lock***

AE lock range control register.

Setting range of awb_lock is 00h to FFh.
If awb_lock has low value, awb lock range will be smaller.
However, small value of awb_lock may cause AWB oscillation

▷ ***AWB_speed***

If awb_speed have high value, AWB speed will be faster.
However, high awb speed value may cause AE oscillation.

(1141~1144) AWB gain min/max clamping reference

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1141	75	awb_rgain_min	0	00	00000000	RW	5	0	AWB gain clamping control
1142	76	awb_rgain_max	255	FF	11111111	RW	5	0	
1143	77	awb_bgain_min	0	00	00000000	RW	5	0	
1144	78	awb_bgain_max	255	FF	11111111	RW	5	0	

▷ ***AWB_r/bgain_min/max***

AWB gain min/max clamping

00h < *awb_rgain_min* < *awb_rgain_max* < FFh
00h < *awb_bgain_min* < *awb_bgain_max* < FFh

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(1177~1178) Total gain

address		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1177	99	totalgain_h	0	00	00000000	RW	6	autov	Total gain
1178	9A	totalgain_l	1	01	00000001	RW	6	autov	

▷ ***totalgain***

totalgain = linear_gain x digitalgain

▶ Register Tables (Detailed) : Group F

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(1284)Parking Guide Line control 0

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1284	04	pg_control0	9	09	00001001	RW	6	aev	Embedded parking guide line control

register name : pg_control0								
register #	bit#	name	default	**9**	default(h)	**09**	default(b)	**00001001**
1284d (04h)	7	x	0	Reserved				
	6	pg_blink	0	Parking guide line blink 0b : disable 1b : enable				
	5	x	0	Reserved				
	4	pg_hlight	0	all pg hlight enable				
	3	x	1	Reserved				
	2	pg_rm	0	remove left side of PG				
	1		0	remove right side of PG				
	0	pg_enable	1	PG enable 0b: disable 1b: enable				

▷ ***pg_hlight***

Total high light zone can be enable/disable at embedded parking guide line.

▷ ***pg_rm***

pg_control0[2] : removing left side of PG ‘1b’ : removing, ‘0b’ : don’t removing

pg_control0[1] : removing right side of PG ‘1b’ : removing, ‘0b’ : don’t removing

▷ ***pg_enable***

PG is enable /disable by pg_control0[0] register bit.

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(1288~1320)Embedded Parking Guide Line

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1288	08	pg_yt	127	7F	01111111	RW	6	aev	Embedded parking guide line control
1289	09	pg_y1	115	73	01110011	RW	6	aev	
1290	0A	pg_y2	2	02	00000010	RW	6	aev	
1291	0B	pg_y3	8	08	00001000	RW	6	aev	
1292	0C	pg_y4	15	0F	00001111	RW	6	aev	
1293	0D	pg_y5	25	19	00011001	RW	6	aev	
1294	0E	pg_y6	37	25	00100101	RW	6	aev	
1295	0F	pg_y7	40	28	00101000	RW	6	aev	
1296	10	pg_y8	56	38	00111000	RW	6	aev	
1297	11	pg_y9	78	4E	01001110	RW	6	aev	
1298	12	pg_y10	82	52	01010010	RW	6	aev	
1299	13	pg_a	143	8F	10001111	RW	6	aev	
1300	14	pg_b	100	64	01100100	RW	6	aev	
1301	15	pg_c	191	BF	10111111	RW	6	aev	
1302	16	pg_d	7	07	00000111	RW	6	aev	
1303	17	pg_e	12	0C	00001100	RW	6	aev	
1304	18	pg_f	21	15	00010101	RW	6	aev	
1305	19	pg_line1	33	21	00100001	RW	6	aev	
1306	1A	pg_line2	35	23	00100011	RW	6	aev	
1307	1B	pg_line3	36	24	00100100	RW	6	aev	
1308	1C	pg_line4	70	46	01000110	RW	6	aev	
1309	1D	pg_line5	72	48	01001000	RW	6	aev	
1310	1E	pg_line6	66	42	01000010	RW	6	aev	
1311	1F	pg_line7	75	4B	01001011	RW	6	aev	
1312	20	pg_line8	113	71	01110001	RW	6	aev	
1313	21	pg_line9	99	63	01100011	RW	6	aev	
1314	22	pg_line10	116	74	01110100	RW	6	aev	
1315	23	pg_center_h	1	01	xxxxxx01	RW	6	aev	
1316	24	pg_center_l	104	68	01101000	RW	6	aev	
1317	25	pg_l_type_h	1	01	xxxxxx01	RW	6	aev	
1318	26	pg_l_type_l	33	21	00100001	RW	6	aev	
1319	27	pg_hl_en_h	0	00	xxxxxx00	RW	6	aev	
1320	28	pg_hl_en_l	0	00	00000000	RW	6	aev	

▷ ***pg_yt***

The boundary of straight line and a curve

▷ ***pg_y1/10***

The start position of 10 points

▷ ***pg_a***

X-axis Start point, X-axis value = 2x(pg_a), Min=01h

▷ ***pg_b***

The slope of embedded parking guide line.

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(1288~1320)Embedded Parking Guide Line

▷ *pg_c*

The weight of slope.

▷ *pg_d*

Embedded parking guide line Width (Min : 04h)

▷ *pg_e*

Embedded parking guide line width weight.

▷ *pg_f*

long line width

▷ *pg_line1/10*

The information decision of each dot line
pg_line1~10 (7): line type ➔ '0': short line width
'1': long line width
pg_line1~10 [6:5]: palette color information of line
➔ palette number 0~3
pg_line1~10 [4:0]: height of each line.

▷ *pg_center*

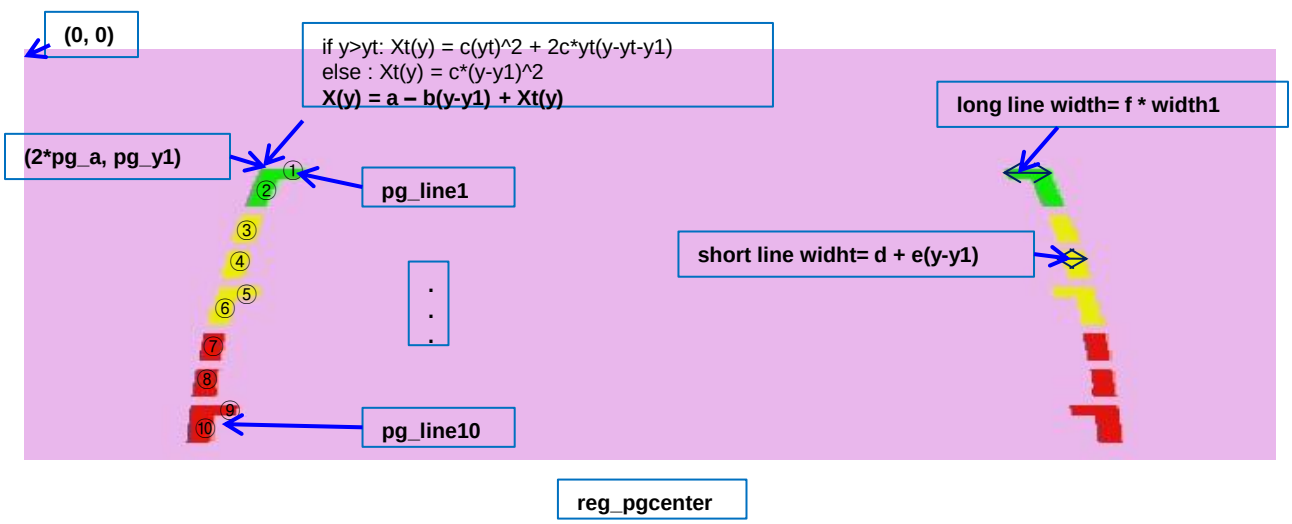
It defines the center position of embedded parking guide line.

▷ *pg_l_type*

Set to type of each line의
'0': width type1(reg_d + e(y-y1) , '1': width type2(reg_f*width1)

▷ *pg_hl_en*

Highlight zone of each line enable/disable



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(1288~1320)Embedded Parking Guide Line

▷ ***Embedded Parking Guide Line condition.***

1. **It can be expression to 10 dot line.(max)**
2. **Each dotted line is the y coordinate of the starting point should be lower than the top line.**
   pg_y1+line1_height(pg_line1[4:0]+1) < pg_y2 ···line9_height(pg_line9[4:0]+1) < pg_y10
3. **PG image from top to bottom, should be increasingly wider.**
4. **The left and right line should be separated more than the minimum 8pixel line.**

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(1435) OSD blink frame

#		register name	default value			type	stage	update	Description
Dec	hex		dec	hex	bin				
1435	9B	blink_frame	0	00	00000000	RW	5	0	OSD blink control

▷ **OSD blink control**

blink_frame speed control.

pg_control0[6] : blink enable

(1437) OSD boundary

#		register name	default value			type	stage	update	Description
Dec	hex		dec	hex	bin				
1437	9D	spi_osd_bndry	0	00	00000000	RW	5	0	OSD boundary

▷ **OSD boundary**

Boundary thickness control.

***spi_osd_bndry[7:6]* : OSD boundary**

OSD layer0 boundary = 0d : no boundary
OSD layer0 boundary = 1d : 1pixel boundary
OSD layer0 boundary = 2d : 2pixel boundary
OSD layer0 boundary = 3d : 3pixel boundary

▶ Register Tables (Detailed) : Group G

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(1540~1551) CCIR656 control

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1540	04	sync_blankEAV_f0	182	B6	10110110	RW	5	0	Blank EAV for field0 of CCIR656 data or blank EAV for frame data
1541	05	sync_blankSAV_f0	171	AB	10101011	RW	5	0	Blank SAV for field0 of CCIR656 data or blank SAV for frame data
1542	06	sync_activeEAV_f0	157	9D	10011101	RW	5	0	Active EAV for field0 of CCIR656 data or active EAV for frame data
1543	07	sync_activeSAV_f0	128	80	10000000	RW	5	0	Active SAV for field0 of CCIR656 data or active SAV for frame data
1544	08	sync_blankEAV_f1	241	F1	11110001	RW	5	0	blank EAV for field1 of CCIR656 data
1545	09	sync_blankSAV_f1	236	EC	11101100	RW	5	0	blank SAV for field1 of CCIR656 data
1546	0A	sync_activeEAV_f1	218	DA	11011010	RW	5	0	Active EAV for field1 of CCIR656 data
1547	0B	sync_activeSAV_f1	199	C7	11000111	RW	5	0	Active SAV for field1 of CCIR656 data
1548	0C	sync_CCIR_FF	255	FF	11111111	RW	5	0	CCIR data format
1549	0D	sync_CCIR_00	0	00	00000000	RW	5	0	
1550	0E	sync_CCIR_80	128	80	10000000	RW	5	0	
1551	0F	sync_CCIR_10	16	10	00010000	RW	5	0	

▷ CCIR656 sync index value

EAV and SAV data value for synchronization.

Address	Name	Description
05, 09h	*BlankSAV*	Blank Range Start of Video
04, 08h	*BlankEAV*	Blank Range End of Video
06, 0Ah	*ActiveEAV*	Active Range End of Video
07, 0Bh	*ActiveSAV*	Active Range Start of Video

▷ sync_ccirFF

CCIR data format FFh

▷ sync_ccir00

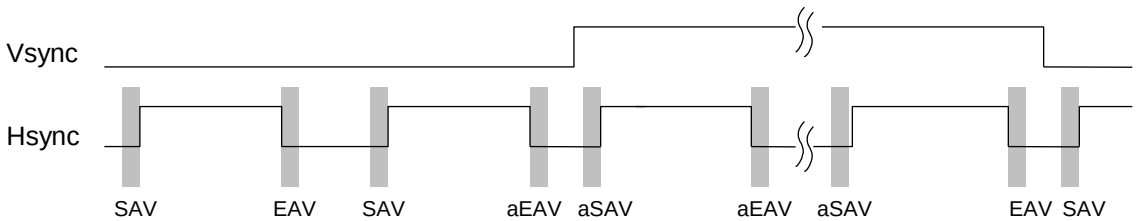
CCIR data format 00h

▷ sync_ccir80

CCIR data format 80h

▷ sync_ccir10

CCIR data format 10h



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... 80 10 80 10 80 10 80 10 FF 00 00 XY ... FF 00 00 XY 80 10 80 10 80 10 80 10

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(1560) OSD transparency

#		register name	default value			type	stage	update	Description
Dec	hex		dec	hex	bin				
1560	18	osd_opac	16	10	xxx10000	RW	5	0	OSD transparency

▷ **OSD transparency**

OSD transparency control.

0d~16d, when set as 16d, OSD image is most opaque .

(1562~1573) palette 1~ 4

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1562	1A	palette_1_y	144	90	10010000	RW	5	0	Palette_1
1563	1B	palette_1_cb	53	35	00110101	RW	5	0	
1564	1C	palette_1_cr	34	22	00100010	RW	5	0	
1565	1D	palette_2_y	210	D2	11010010	RW	5	0	Palette_2
1566	1E	palette_2_cb	16	10	00010000	RW	5	0	
1567	1F	palette_2_cr	146	92	10010010	RW	5	0	
1568	20	palette_3_y	81	51	01010001	RW	5	0	Palette_3
1569	21	palette_3_cb	90	5A	01011010	RW	5	0	
1570	22	palette_3_cr	240	F0	11110000	RW	5	0	
1571	23	palette_4_y	16	10	00010000	RW	5	0	Palette_4
1572	24	palette_4_cb	128	80	10000000	RW	5	0	
1573	25	palette_4_cr	128	80	10000000	RW	5	0	

▷ **palette1~3**

Y/CB/CR value for OSD color.

▷ **palette4**

Y/CB/CR value for horizontal boundary of OSD line.

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(1693) Encoder control 1

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1693	9D	enc_control1	0	00	00000000	RW	5	0	Encoder control

register name : enc_control1								
register #	bit#	name	default	**0**	default(h)	**00**	default(b)	**00000000**
1693d (9Dh)	7	x	0	reserved				
	6	x	0	reserved				
	5	x	0	reserved				
	4	x	0	reserved				
	3	enc_chroma_kill	0	TV encoder chroma signal kill enable@led ON(BW_mode) 0b : disable 1b : enable				
	2	burst kill	0	TV encoder color burst kill enable@led ON(BW_mode) 0b : disable 1b : enable				
	1	x	0	reserved				
	0	x	0	reserved				

▷ **enc_chroma_kill**

0b : disable
1b : chroma signal kill@ led on

▷ **burst_kill**

0b : disable
1b : burst kill @ led on

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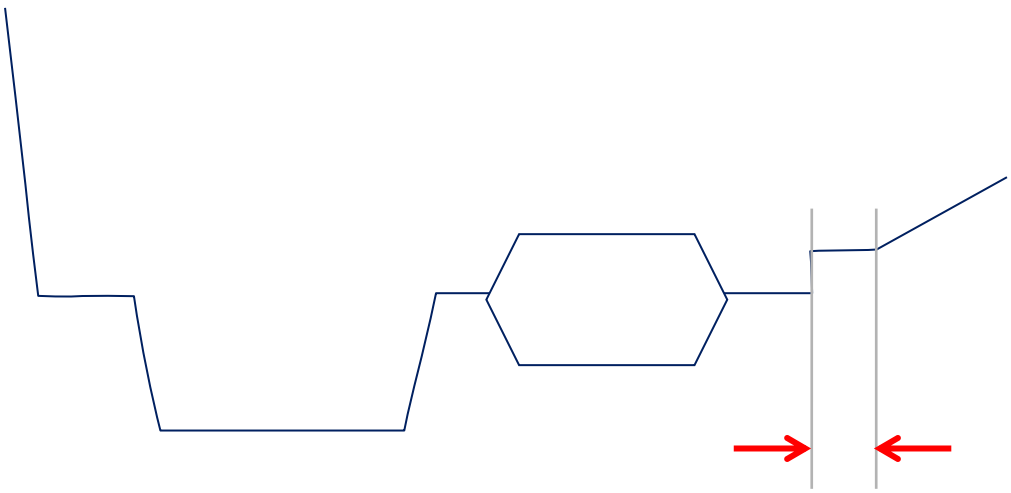
(1705) Setup time width

#		register name	default value			type	stage	update	Description
Dec	hex		dec	hex	bin				
1705	A9	setup_w	7	07	xxx00111	RW	5	0	Setup time width

▷ ***setup_w***

Setup time width control register.



setup_w

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(1706~1710) horizontal sync control of composite signal

#		register name	default value			type	stage	update	Description
Dec	hex		dec	hex	bin				
1706	AA	hsync_p_toffset	0	00	xxx00000	RW	5	0	Stop point of hsync
1707	AB	burst_duration	0	00	00000000	RW	5	0	Burst duration
1708	AC	burst_slope_step	56	38	00111000	RW	5	0	
1709	AD	l_blank_start	0	00	00000000	RW	5	0	Line blanking interval
1710	AE	l_blank_stop	0	00	00000000	RW	5	0	

▷ ***hsync_p_toffset***

Hsync stop point can be 1 clock(pclk)unit control.
hsync stop point = ref_stop_point + *hsync_p_toffset[3:0]* :when hsync_p_toffset[4]='0'
hsync stop point = ref_stop_point - *hsync_p_toffset[3:0]* :when hsync_p_toffset[4]='1'

▷ ***burst_duration***

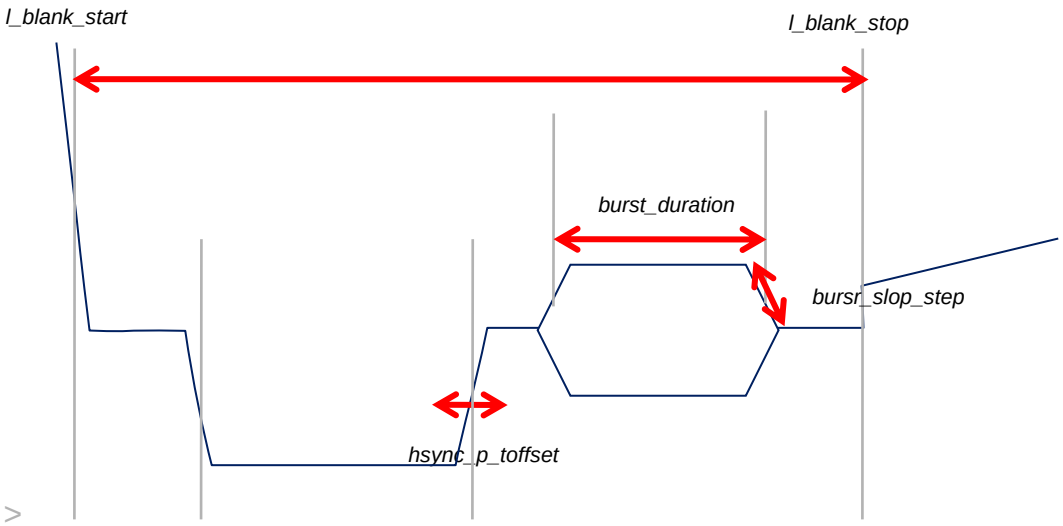
Burst duration can be 1 clock(pclk)unit control.
burst duration = ref_duration + *burst_duration[6:0]* :when *burst_duration[7]*='0'
burst duration = ref_duration - *burst_duration[6:0]* :when *burst_duration[7]*='1'

▷ ***burst_slope_step***

Burst envelop rising or falling time can be 1 clock(pclk)unit control.
envelop = 0 : start point
envelop = 511 when envelop+ *burst_slop_step* >511 else
envelop = envelop+*burst_slop_step*

▷ ***l_blank_start/stop***

Line blanking interval start/stop point control.
line blanking interval start= ref_start_point+*l_blank_start*
line blanking interval stop= ref_stop_point - *l_blank_stop*



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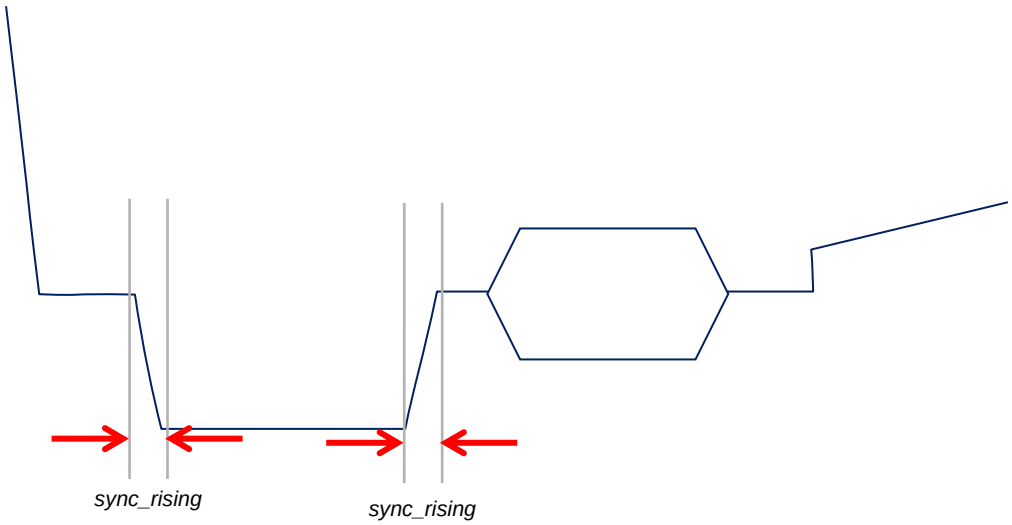
(1711) control rise time of composite horizontal sync

#		register name	default value			type	stage	update	Description
Dec	hex		dec	hex	bin				
1711	AF	sync_rising	1	01	xxxx0001	RW	5	0	horizontal rising time control of composite signal

▷ ***sync_rising***

Horizontal sync rising time can be 0~15color(pclk)unit control.



(1712) resolution enhance gain

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1712	B0	resol_gain	8	08	00001000	RW	5	0	Resolution enhance gain

▷ ***resol_gain***

At the TV encoder block, adjust the sharpness of the high frequency edge.

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(1719) Encoder mode

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1719	B7	enc_mode	u	u	uuuuuuuu	RW	5	0	Encoder mode

▷ ***enc_mode[1:0]***

"00" : (M) NTSC, NTSC-J, NTSC-4.43

"01" : (B, D, G, H, I, N) PAL

"10" : (Nc) PAL

"11" : (M) PAL

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(1720~1735) Composite level parameters

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1720	B8	enc_sync	16	10	00010000	RW	5	0	Encoder sync level
1721	B9	enc_blankH	0	00	00000000	RW	5	0	Encoder blank level
1722	BA	enc_blankL	u	u	uuuuuuuu	RW	5	0	
1723	BB	enc_pedestal	u	u	uuuuuuuu	RW	5	0	Encoder pedestal
1724	BC	enc_burst	u	u	uuuuuuuu	RW	5	0	Burst amplitude
1725	BD	enc_Ygain	u	u	uuuuuuuu	RW	5	0	Y convergence gain from YCbCr to YUV
1726	BE	enc_Ugain	u	u	uuuuuuuu	RW	5	0	U convergence gain from YCbCr to YUV
1727	BF	enc_Vgain	u	u	uuuuuuuu	RW	5	0	V convergence gain from YCbCr to YUV
1728	C0	enc_Yrange_H	3	03	xxxxx011	RW	5	0	Max. luminance
1729	C1	enc_Yrange_L	32	20	00100000	RW	5	0	
1730	C2	enc_Crange_H	1	01	xxxxx001	RW	5	0	Max. amplitudes of chrominance
1731	C3	enc_Crange_L	u	u	uuuuuuuu	RW	5	0	
1732	C4	enc_chroma_max_H	3	03	xxxxx011	RW	5	0	Maximum chrominance of composite output
1733	C5	enc_chroma_max_L	u	u	uuuuuuuu	RW	5	0	
1734	C6	enc_chroma_min_H	0	00	xxxxx000	RW	5	0	Minimum chrominance of composite output
1735	C7	enc_chroma_min_L	u	u	uuuuuuuu	RW	5	0	

▷ ***enc_sync***

Encoder sync level

▷ ***enc_blank***

Encoder blank level

▷ ***enc_pedestal***

Encoder pedestal level

▷ ***enc_burst***

Burst amplitude

▷ ***enc_Y/U/Vgain***

Conversion gain of YCbCr to YUV

▷ ***enc_Yrange***

Separate Y range into positive and negative regions.

▷ ***enc_Crange***

Define maximum level of Chrominance.

▷ ***enc_chroma_max***

Define maximum level of Composite.

▷ ***enc_chroma_min***

Define minimum level of Composite.

default value : U ➔ wire-strapping register

Refer to next page

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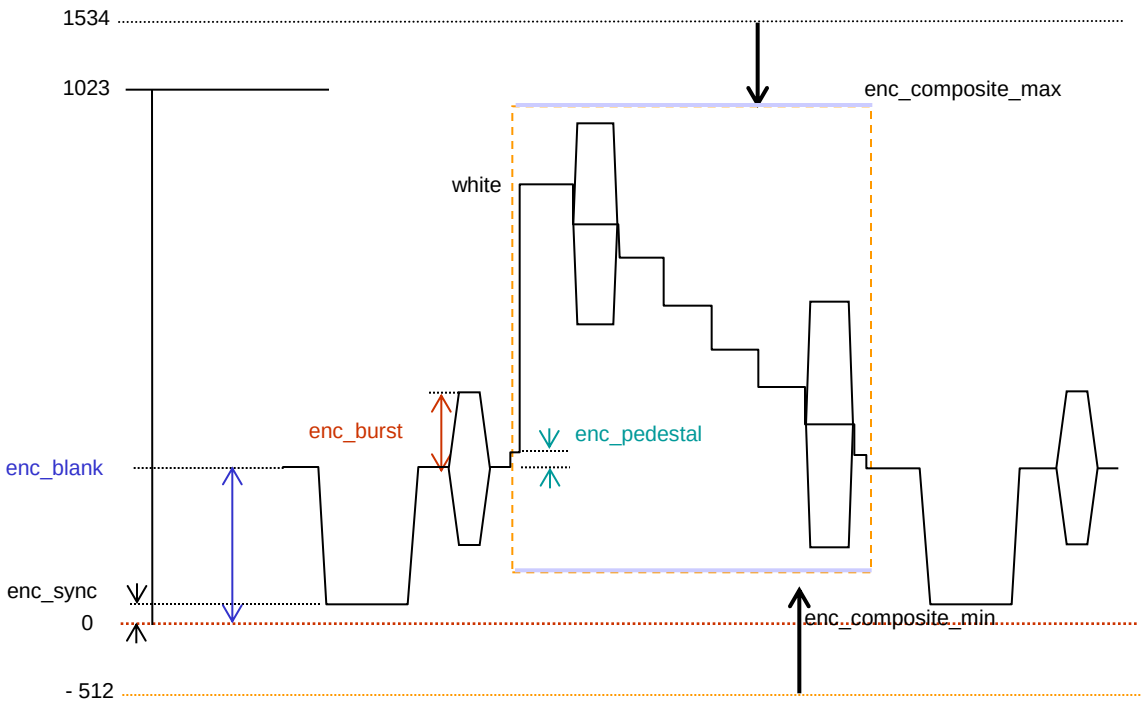
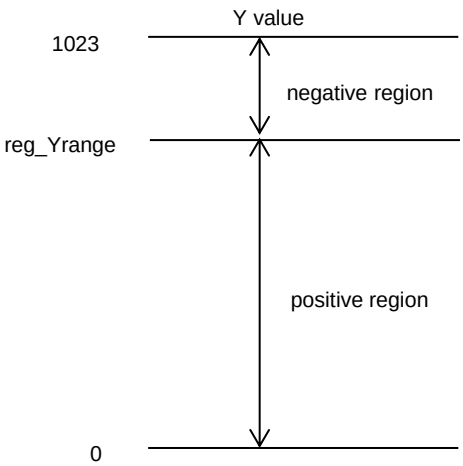
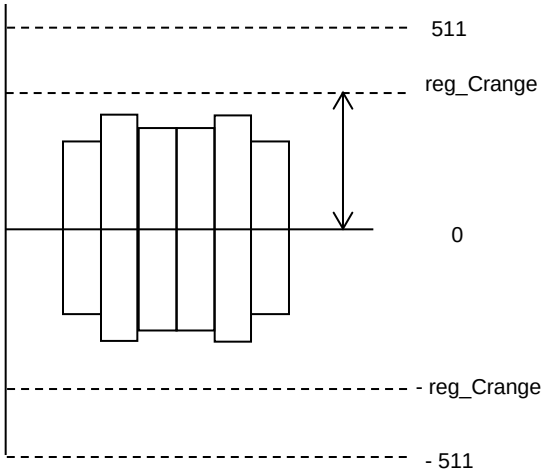


reg_enc_composite_max/min registers define the max. and min. of active data level.



reg_Yrange defines the boundary between positive or negative number of Y before composition.
In colorbar, Y might be negative values. It is the reason why the register exists.



reg_Crange designates the maximum amplitude of chroma. It can be one of 0 to 511.

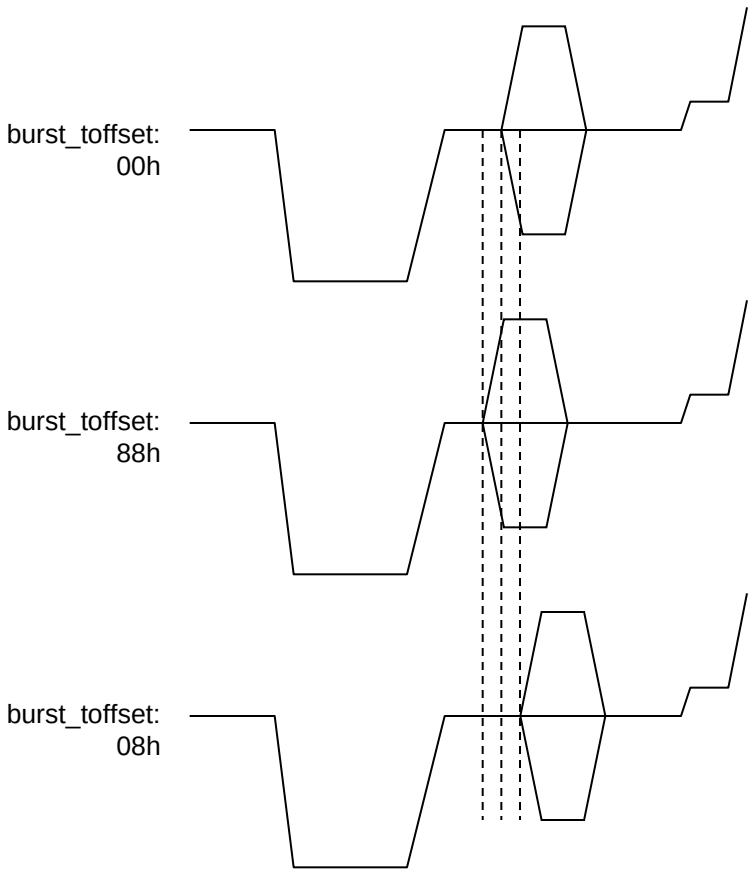
(1766) Burst time offset

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1766	E6	burst_toffset	0	00	00000000	RW	5	0	Burst time +/- offset

▷ ***burst_toffset***

Change the location of the color burst.

msb: sign, other bits : magnitude



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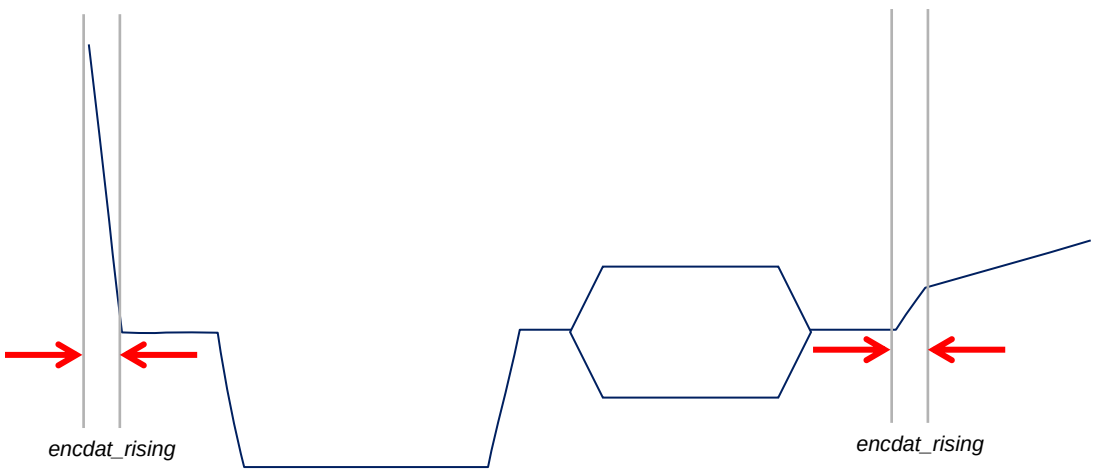
(1771) control rise time of composite horizontal sync

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1771	EB	encdat_rising	1	01	xxxx0001	RW	5	0	edge of the line blanking pulse rising time control

▷ ***encdat_rising***

edge of the line blanking pulse rising time can be 0~15 (0Fh)clock(pclk)unit control.



1/4 inch NTSC/PAL CMOS Image Sensor with 640 X 480 Pixel Array

(1772) Sub-carrier frequency control

#		register name	default value			type	stage	update	Description
dec	hex		dec	hex	bin				
1772	EC	enc_scfreq	u	u	uuuuuuuu	RW	5	0	Subcarrier frequency selection for which TV mode

▷ ***enc_scfreq***

default value : U ➔ wire-strapping register

Subcarrier frequency selection for which TV mode.

"00" : 3.579545 MHz for (M) NTSC, NTSC-J

"01" : 4.43361875 MHz for (B, D, G, H, I, N) PAL

"10" : 3.58205625 MHz for (Nc) PAL

"11" : 3.57561149 MHz for (M) PAL

C= U*sin(ωt) + V*cos(ωt)