OV528-B64 Serial Bus Camera System

Single-Chip Camera to Serial Bridge

General Description

The OV528 Serial Bus Camera system is a low cost, low powered single chip solution for high-resolution serial bus PDA/cellular phone camera accessory applications. Combined with the OV76x0/OV66x0 CMOS VGA/CIF CAMERACHIPS™, the OV528 comprises a low cost, highly integrated serial camera system with no additional DRAM required.

The OV528 can be attached to a wireless or PDA host and performs as a video camera or a JPEG-compressed still camera. When performing as a video camera, the TFT-LCD panel of the host operates as a viewfinder. Users can send out a snapshot command from the host in order to capture a full resolution single frame still picture that is compressed by the JPEG engine and transfer it to the host.

Features

- Low cost single chip
- Low power consumption
- Low voltage 2.5V (Core) and 3.3 V (I/O) operation
- No additional DRAM required
- Built-in JPEG compression engine
  - JPEG CODEC with variable quality settings for different resolutions
- RS-232 serial interface and 4-wire serial bus
- Built-in PLL
- Built-in microcontroller
- User controlled General Purpose I/O pins
- Down-sampling, Clamping, and Windowing (DCW) functions
- Color conversion circuitry for 4 gray/16 gray/256 gray/12-bit RGB/16-bit RGB/Pallet 256 RGB preview images

Ordering Information

Product	Package
OV528-B64	BGA-64

Applications

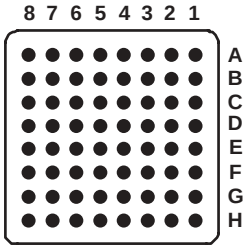
- Serial bus PDA/cellular applications combined with the following OmniVision CAMERACHIP families:
  - OV76x0/OV71x0 (VGA)
  - OV66x0/OV61x0 (CIF)

NOTE: The OV528 supports digital image sensors up to VGA resolution. However, it will not support analog image sensors (OVx9xx or OVx4xx products)

Key Specifications

Power Supply	**Core**	2.5 V
	I/O	3.3 V
Power Requirements	**Active**	55 mA
	Standby	90 µA
Temperature Range		0°C to 70°C
Package Dimensions		8.00 mm x 8.00 mm

Figure 1 OV528-B64 Pin Diagram



	8	7	6	5	4	3	2	1
A	GPIO0[3]	ID1	IO_VDD4	DUMP_PRC	CORE_VSS2	ID3	GPIO0[7]	GPIO1[0]
B	TEST	ID2	GPIO0[6]	SEL_UART_	SCS_	SIO1	Y0	IO_VDD5
C	SNAP_	EA_	ID0	IO_VSS3	CORE_VDD2	SIO0	GPIO1[1]	Y1
D	IO_VDD3	XOUT	XIN	IO_VSS1	IO_VSS2	GPIO1[2]	Y2	GPIO1[3]
E	RXD	CTS_	TXD	IO_VSS6	IO_VSS5	IO_VSS4	Y3	Y5
F	P2[0]	IO_VDD2	IO_VSS7	IO_VDD1	CORE_VDD1	Y4	IO_VDD6	Y6
G	RTS_	UCO_I	SXOUT	RESET_	CORE_VSS1	HREF	PLL_SEL	Y7
H	UCLK	GPIO0[1]	SXIN	MCLK_SEL	VSYNC	CCLK	IO_VDD7	PCLK

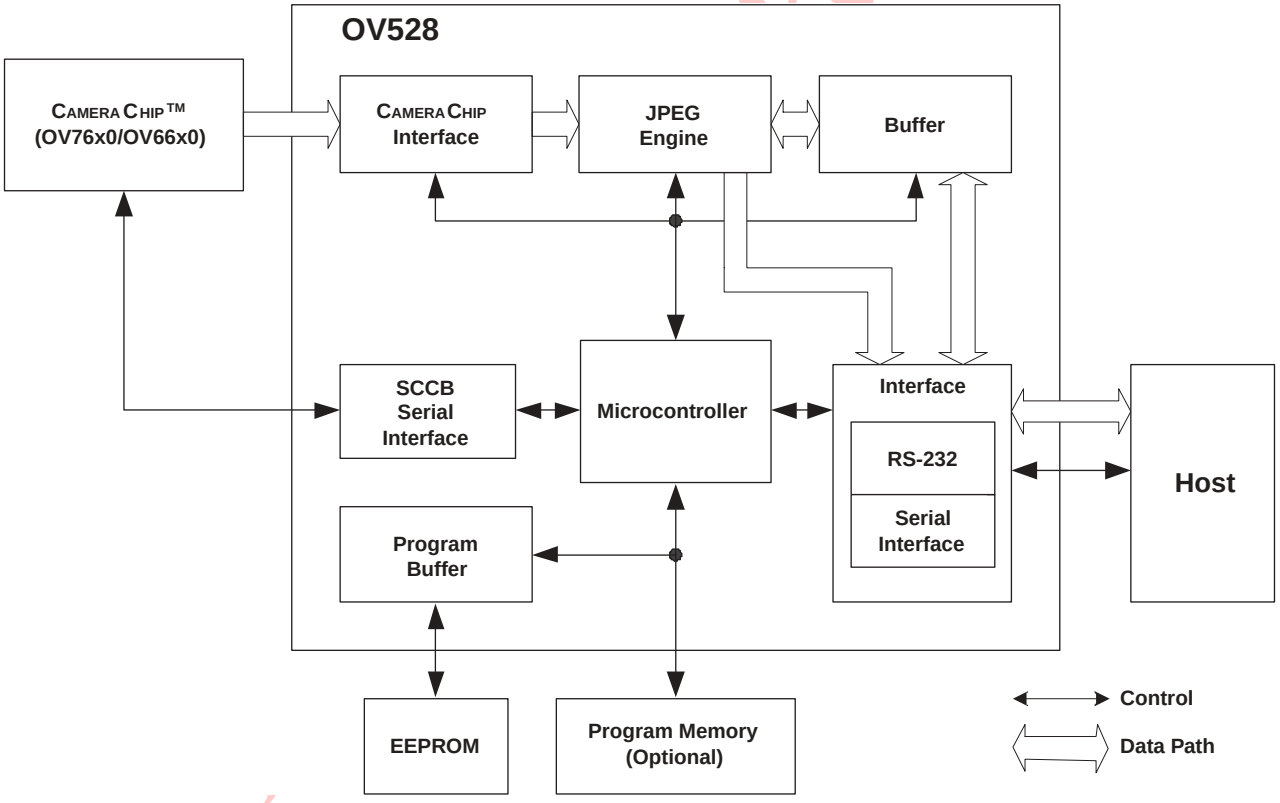
Functional Description

Figure 2 shows the functional block diagram of the OV528 CAMERAMATE single-chip processor. The OV528 includes:

- Microcontroller
- CameraChip Interface
- JPEG Compression Engine
- Program Buffer
- SCCB Serial Interface
- Serial Interfaces
  - RS-232 Serial Interface
  - 4-Wire Serial Bus
- Miscellaneous Functions

The OV528 supports an external EEPROM and optional program memory (as shown in Figure 2).

Figure 2 Functional Block Diagram



Microcontroller

The Microcontroller operates as an embedded controller only and can be programmed by the user if custom applications are desired. Contact OmniVision for further information on the Microcontroller implementation.

CAMERACHIP Interface

The CAMERACHIP interface supports the OV76x0/OV66x0 color image sensors with the 8-bit YCbCr interface. The CAMERACHIP interface has built-in Down-sampling, Clamping, and Windowing (DCW) circuitry for VGA/CIF/SIF/QCIF/160x128/80x64 image resolutions. It also has built-in color conversion circuitry for 4 gray/16 gray/256 gray/12-bit RGB/16-bit RGB/Pallet 256 RGB preview images.

JPEG Compression Engine

The OV528 uses JPEG CODEC with variable quality settings for various resolutions.

Program Buffer

Program memory is required for the embedded microcontroller to respond to host commands correctly, as well as to store all necessary parameters for adjusting image/compression qualities. A serial type program memory is required for the OV528. The content of the program memory can be updated on the fly.

SCCB Serial Interface

The SCCB serial interface controls the CAMERACHIP operation as well as interfacing directly to the Microcontroller. In all cases, the OV528 is considered the SCCB 'Master' and all other SCCB devices, such as the CAMERACHIP, are designated as 'Slaves'.

Serial Interfaces

RS-232 Serial Interface

The OV528 uses an RS-232 serial interface for transferring JPEG still pictures or 160 x 128 preview images at 8 bpp with 0.75 to 6 frames per second (fps). The RS-232 interface is capable of 115.2 to 920 Kbps transfer rate

4-Wire Serial Bus

The OV528 also has a 4-wire serial bus for transferring JPEG still pictures or SIF (320 x 240) preview images at 4 bpp with 6 to 8 fps. The 4-wire serial bus is capable of 1 to 2 Mbps transfer rate.

Miscellaneous Functions

Other miscellaneous functions of the OV528 are:

- Eight General Purpose I/O pins
- Built-in PLL

Pin Description

Table 1 Pin Description by Function

Pin Number	Name	Pin Type	Function/Description
Camera Interface			
H3	CCLK	Output	Camera clock output
G3	HREF	Input	Camera horizontal window reference input
H4	VSYNC	Input	Camera vertical sync input
B2	Y0	Input	Camera Y/Cb/Cr inputs
C1	Y1		
D2	Y2		
E2	Y3		
F3	Y4		
E1	Y5		
F1	Y6		
G1	Y7		
H1	PCLK	Input	Camera pixel clock input
Serial Camera Control Bus (SCCB) Interface			
B4	SCS_	Output	SCCB chip select output
B3	SIO1	Output	SCCB control signal 1
C3	SIO0	I/O	SCCB control signal 0
Serial Interface			
G8	RTS_	I/O	Request to send I/O signal
E7	CTS_	Input	Clear to send input signal
E8	RXD	Input	Serial input
E6	TXD	Output	Serial output
Clock and Reset			
G2	PLL_SEL	Input	PLL select
G5	RESET_	Input	Power-on reset input, active low.
G6	SXOUT	Output	Serial bus crystal output
H6	SXIN	Input	Serial bus crystal input
H8	UCLK	Output	RS-232 master clock output
D6	XIN	Input	System crystal input
D7	XOUT	Output	System crystal output

Table 1 Pin Description by Function (Continued)

Pin Number	Name	Pin Type	Function/Description
Serial Program Identification			
C6	ID0	I/O	Serial program memory ID bit[3:0]
A7	ID1		
B7	ID2		
A3	ID3		
General Purpose Input/Output (GPIO)			
H7	GPIO0[1]	I/O	General purpose I/O pins, Port 0, bit[1]
A8	GPIO0[3]	I/O	General purpose I/O pins, Port 0, bit[3]
B6	GPIO0[6]	I/O	General purpose I/O pins, Port 0, bits[7:6]
A2	GPIO0[7]		
A1	GPIO1[0]	I/O	General purpose I/O pins, Port 1, bits[3:0]
C2	GPIO1[1]		
D3	GPIO1[2]		
D1	GPIO1[3]		
Miscellaneous			
H5	MCLK_SEL	Input	Master Clock Select 0: 48 MHz crystal 1: Internal PLL
G7	UCO_I	Input	External/Internal Microcontroller Select 0: Internal microcontroller *Note: Must select internal microcontroller.*
C8	SNAP_	Input	Snapshot button input, active low.
B8	TEST	Input	Test Mode Enable 0: Disabled 1: Enabled
A5	DUMP_PRC	Input	Host Programming Enable 0: Disabled 1: Enabled
B5	SEL_UART_	Input	Serial Bus Select 0: RS-232
Internal Microcontroller I/O Ports			
F8	P2[0]	I/O	Internal Microcontroller Port 2 bit 0
C7	EA_	I/O	Internal Microcontroller EA_

Table 1 Pin Description by Function (Continued)

Pin Number	Name	Pin Type	Function/Description
Power and Ground			
H2	IO_VDD7	DVDD	Digital 3.3V power
F5	IO_VDD1		
F7	IO_VDD2		
D8	IO_VDD3		
A6	IO_VDD4		
B1	IO_VDD5		
F2	IO_VDD6		
F4	CORE_VDD1	CVDD	Digital 2.5V power
C4	CORE_VDD2		
C5	IO_VSS1	DVSS	Digital ground
D4	IO_VSS2		
D5	IO_VSS3		
E3	IO_VSS4		
E4	IO_VSS5		
E5	IO_VSS6		
F6	IO_VSS7		
G4	CORE_VSS1	CVSS	Digital ground
A4	CORE_VSS2		

Electrical Characteristics

Table 2 Operating Conditions

Parameter	Min	Max	Unit
Operating temperature	0	40	°C
Storage temperature	-40	125	°C
Operating humidity	TBD	TBD	
Storage humidity	TBD	TBD	

Table 3 Absolute Maximum Ratings

Ambient Storage Temperature	-40ºC to +125ºC
All Input/Output Voltages (with respect to Ground)	-0.3 V to VDD_IO+1 V
Lead Temperature, Surface-mount process	+230ºC
ESD Rating, Human Body model	2000 V

NOTE: Exceeding the Absolute Maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent device damage.

Table 4 DC Characteristics (V_{DD} = 3.3V ± 10%, T_A = 0º to 125ºC)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input voltage HIGH	CMOS	0.7 x V_{DD}			V
V_{IH}	Input voltage HIGH	TTL	2.0			V
V_{IL}	Input voltage LOW	CMOS			0.3 x V_{DD}	V
V_{IL}	Input voltage LOW	TTL			0.8	V
V_{OH}	Output voltage HIGH		2.4		V_{DD}	V
V_{OL}	Output voltage LOW			0.2	0.4	V
I_S	SUSPEND mode current	SUSPEND		90		µA
I_{DDA}	Normal operating current	Operating		55		mA

Timing Specifications

SCCB Interface Timing

Figure 3 SCCB Timing Diagram

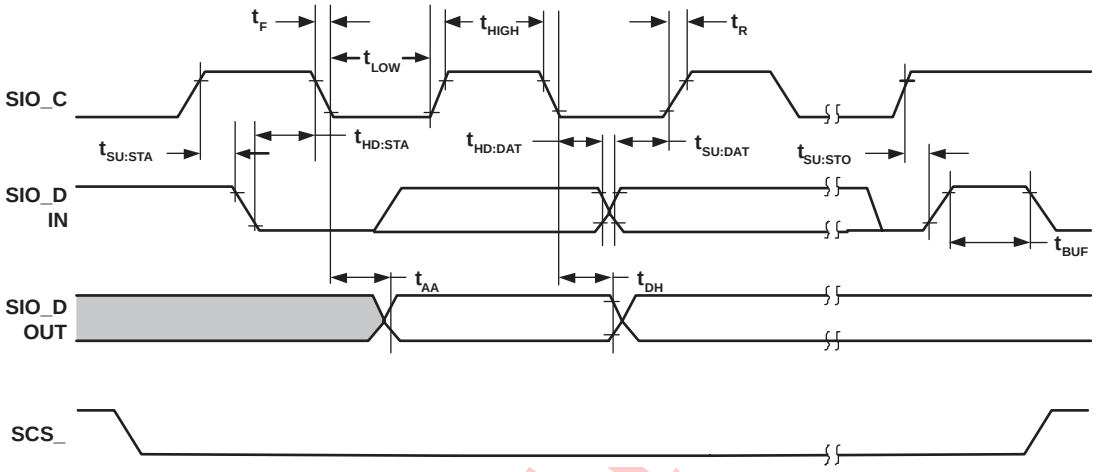


Table 5 SCCB Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
f_{SIO_C}	Clock Frequency			400	KHz
t_{LOW}	Clock Low Period	1.3			µs
t_{HIGH}	Clock High Period	600			ns
t_{AA}	SIO_C low to Data Out valid	100		900	ns
t_{BUF}	Bus free time before new START	1.3			µs
$t_{HD:STA}$	START condition Hold time	600			ns
$t_{SU:STA}$	START condition Setup time	600			ns
$t_{HD:DAT}$	Data-in Hold time	0			µs
$t_{SU:DAT}$	Data-in Setup time	100			ns
$t_{SU:STO}$	STOP condition Setup time	600			ns
$t_{R,}$ t_F	SCCB Rise/Fall times			300	ns
t_{DH}	Data-out Hold time	50			ns

Register Set

Table 6 provides a list and description of the Device Control registers contained in the OV528.

Table 6 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00	CID	28	RW	Chip ID
01	HSB	01	RW	Horizontal Start Byte of Image Windowing
02	VSB	01	RW	Vertical Start Byte of Image Windowing
03	HPL	A0	RW	Horizontal Pixel Length Pixel Length = HPL x 4 (default horizontal pixel length is 640)
04	VPL	78	RW	Vertical Pixel Length Pixel Length = VPL x 4 (default vertical pixel length is 480)
05	PLC	03	RW	Polarity Control Bit[7:3]: Reserved Bit[2]: PCLK Bit[1]: HREF Bit[0]: VSYNC 0: Inverted 1: Normal
06	IDC	81	RW	Image Disable Counter Bit[7]: Enable Bit[6:0]: Image disable counter After starting sensor, users can decide how many frames to discard before capturing.
07	RSVD	XX	–	Reserved
08	JPC	00	RW	JPEG Control Bit[7]: Global JPEG enable 0: Disable 1: Enable Bit[6]: JPEG decoder enable 0: Disable 1: Enable Bit[5:1]: JPEG control setting Bit[0]: JPEG encoder enable 0: Disable 1: Enable Only use the following values: 00h: Update quantization table 9Fh: Encoding BEh: Stop encoding C2h: Decoding 82h: Stop decoding

Table 6 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
09	PVC	00	RW	Preview Control Bit[7]: Snapshot button status (Read only) 00h: Stop 3Fh: Start
0A	HBB	28	RW	Buffer Transfer Size - high byte (Real_Size/2)
0B	LBB	15	RW	Buffer Transfer Size - low byte (Real_Size/2)
0C	SBC	1F	RW	Serial Bus Control Bit[7]: RTS_ polarity control 0: Inverted 1: Normal Bit[6]: Phase control Bit[5]: Bit ordering 0: Low bit first 1: High bit first Bit[4]: TXD/RXD polarity control 0: Inverted 1: Normal Bit[3]: Microcontroller program control 0: Normal 1: Download via serial bus Bit[2:0]: Serial bus control enabled/disabled 111: Enabled Others: Disabled
0D	UBR	7F	RW	RS-232 Baud Rate Control Baud Rate = SXIN / 2 / (UBR + 1)
0E	UCLK	01	RW	UCLK Divider 80h: UCLK = XIN for PLL enable UCLK = XIN/4 for PLL disable Others: UCLK = XIN / 2 / (UDIV + 1) PLL enable UCLK = XIN / 8 / (UDIV + 1) PLL disable
0F	CDIV	01	RW	CCLK Divider 80h: CCLK = XIN Others: CCLK = XIN x 2 / (CDIV + 1)

Table 6 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
10	CCC	00	RW	Color Conversion Control Bit[7]: Reserved Bit[6:5]: Down-sampling 00: %1 01: %2 10: %4 11: Reserved Bit[4]: Gray/Color select 0: Gray 1: Color Bit[3:2]: Color select 00: 8-bit color 01: 12-bit color 10: 16-bit color 11: Reserved Bit[1:0]: Gray select 00: 4 gray 01: 16 gray 10: 256 gray 11: Reserved
11	BFC	00	RW	Buffer Control Bit[7]: Reserved Bit[6]: Write buffer failure table 0: Enabled 1: Disabled Bit[5:3]: Buffer access mode 000: JPEG encoder access 011: Microcontroller access 100: JPEG decoder access Others: Reserved Bit[2]: Buffer failure table 0: Disable 1: Enable Bit[1]: Address auto increment 0: Disable 1: Enable Bit[0]: Write/read buffer 0: Write 1: Read
12	BWA	00	RW	Buffer Failure Table Write Address
13	HBWA	00	RW	High Byte Address for Microcontroller to Access Buffer
14	LBWA	00	RW	Low Byte Address for Microcontroller to Access Buffer
15	HBWD	00	RW	Highest Byte of Write Data for Buffer Failure Table
16	MBWD	00	RW	Middle Byte of Write Data for Buffer Failure Table
17	LBWD	00	RW	Lowest Byte of Write Data for Buffer Failure Table

Table 6 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
18	HBRD	–	R	Highest Byte of Read Data for Buffer Failure Table
19	MBRD	–	R	Middle Byte of Read Data for Buffer Failure Table
1A	LBRD	–	R	Lowest Byte of Read Data for Buffer Failure Table
1B	BAC	01	RW	Buffer Access Control Bit[7:3]: Reserved Bit[2]: JPEG decoder access 0: Disable 1: Enable Bit[1]: JPEG encoder access 0: Disable 1: Enable Bit[0]: Microcontroller access 0: Disabled 1: Enabled
1C	HBJPB	00	RW	High Byte Address of JPEG Buffer for Microcontroller Access
1D	LBJPB	00	RW	Low Byte Address of JPEG Buffer for Microcontroller Access
1E	HBJPWD	00	RW	High Byte Write Data of JPEG Buffer for Microcontroller Access
1F	LBJPWD	00	RW	Low Byte Write Data of JPEG Buffer for Microcontroller Access
20	HBJPRD	–	R	High Byte Read Data of JPEG Buffer for Microcontroller Access
21	LBJPRD	–	R	Low Byte Read Data of JPEG Buffer for Microcontroller Access
22	HBBWD	00	RW	High Byte Write Data of Buffer for Microcontroller Access
23	LBBWD	00	RW	Low Byte Write Data of Buffer for Microcontroller Access
24	HBBRD	–	R	High Byte Read Data of Buffer for Microcontroller Access
25	LBBRD	–	R	Low Byte Read Data of Buffer for Microcontroller Access
26	HBSRD	–	R	High Byte Read Data of Serial Bus for Microcontroller Access
27	LBSRD	–	R	Low Byte Read Data of Serial Bus for Microcontroller Access

Table 6 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
28	CHC	00	RW	Chip Control Bit[7:6]: Reserved Bit[5]: JPEG decoding 0: Disable 1: Enable Bit[4]: Serial bus IN control 0: Read Microcontroller commands from the host 1: Read data from the host to buffer Bit[3:2]: Serial bus OUT control 00: Write preview image to the host 01: Write JPEG still picture to the host 10: Write Microcontroller commands to the host 11: Reserved Bit[1:0]: JPEG Encoding/Buffer Transfer 00: Transfer data from the host to buffer 01: Reserved 10: Reserved 11: JPEG encoding
29	HBSWD	00	RW	High Byte Write Data of Serial Bus for Microcontroller Access
2A	LBSWD	00	RW	Low Byte Write Data of Serial Bus for Microcontroller Access
2B	CSD	–	R	Current Data Byte Received from Serial Bus
2C	RSTC	06	W	Reset Control Bit[7:3]: Reserved Bit[2]: Logic reset 0: Reset 1: Normal Bit[1]: System reset 0: Reset 1: Normal Bit[0]: SUSPEND 0: Normal 1: Suspend
2D	RUST	00	RW	Resume Start Time
2E	RUET	00	RW	Resume End Time
2F-47	RSVD	XX	–	Reserved
48	C0	40	RW	R Matrix Y Coefficient R = (C0 x Y) + (C1 x Cr) + (C2 x Cb) + ROF
49	C1	00	RW	R Matrix Cr Coefficient
4A	C2	58	RW	R Matrix Cb Coefficient
4B	ROF	00	RW	R Matrix Offset
4C	C3	40	RW	G Matrix Y Coefficient G = (C3 x Y) + (C4 x Cr) + (C5 Cb) + GOF

Table 6 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
4D	C4	00	RW	G Matrix Cr Coefficient
4E	C5	58	RW	G Matrix Cb Coefficient
4F	GOF	00	RW	G Matrix Offset
50	C6	40	RW	B matrix Y coefficient B = (C6 x Y) + (C7 x Cr) + (C8 Cb) + BOF
51	C7	00	RW	B matrix Cr coefficient
52	C8	58	RW	B matrix Cb coefficient
53	GOF	00	RW	B matrix offset
54	RSTP0	24	RW	R step conversion 0
55	RSTP1	49	RW	R step conversion 1
56	RSTP2	6D	RW	R step conversion 2
57	RSTP3	92	RW	R step conversion 3
58	RSTP4	B6	RW	R step conversion 4
59	RSTP5	DB	RW	R step conversion 5
5A	RSTP6	FF	RW	R step conversion 6
5B	GSTP0	24	RW	G step conversion 0
5C	GSTP1	49	RW	G step conversion 1
5D	GSTP2	6D	RW	G step conversion 2
5E	GSTP3	92	RW	G step conversion 3
5F	GSTP4	B6	RW	G step conversion 4
60	GSTP5	DB	RW	G step conversion 5
61	GSTP6	FF	RW	G step conversion 6
62	BSTP0	55	RW	B step conversion 0
63	BSTP1	AA	RW	B step conversion 1
64	BSTP2	FF	RW	B step conversion 2

Table 6 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
65	CSS	08	RW	Chip Select and Status Bit[7]: Serial bus received FIFO empty status (Read only) Bit[6]: Serial bus received FIFO full status (Read only) Bit[5]: Serial bus transmitted FIFO empty status (Read only) Bit[4]: Serial bus transmitted FIFO full status (Read only) Bit[3]: Reserved Bit[2]: Program memory chip select Bit[1]: Buffer chip select Bit[0]: JPEG buffer chip select
66	HBSRC	–	R	Highest Byte of Serial Bus Received Counter
67	MBSRC	–	R	Middle Byte of Serial Bus Received Counter
68	LBSRC	–	R	Lowest Byte of Serial Bus Received Counter
69	HBSRI	00	RW	Highest Byte of Serial Bus Received Interrupt Counter
6A	MBSRI	00	RW	Middle Byte of Serial Bus Received Interrupt Counter
6B	LBSRI	08	RW	Lowest Byte of Serial Bus Received Interrupt Counter
6C	HBSBTC	–	R	Highest Byte of Serial Bus Transmitted Counter
6D	MBSBTC	–	R	Middle Byte of Serial Bus Transmitted Counter
6E	LBSBTC	–	R	Lowest Byte of Serial Bus Transmitted Counter
6F	HBSBTI	00	RW	Highest Byte of Serial Bus Transmitted Interrupt Counter
70	MBSBTI	00	RW	Middle Byte of Serial Bus Transmitted Interrupt Counter
71	LBSBTI	08	RW	Lowest Byte of Serial Bus Transmitted Interrupt Counter
72	QZC	CC	RW	Quantization Control Bit[7]: Chroma quantization select 0: Without rounding 1: With rounding Bit[6:4]: Chroma quantization bias Bit[3]: Luma quantization select 0: Without rounding 1: With rounding Bit[2:0]: Luma quantization bias
73	SBD	10	RW	Snapshot De-bounce Delay

Table 6 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
74	INT0M	FF	RW	Microcontroller External Interrupt Mask 0 Bit[7]: Buffer overflow interrupt Bit[6]: Serial bus receiving done interrupt Bit[5]: Serial bus transmitting done interrupt Bit[4]: JPEG decoding done interrupt Bit[3]: JPEG encoding done interrupt Bit[2]: Reserved Bit[1]: Image start interrupt Bit[0]: Snapshot interrupt
75	INT0S	–	R	Microcontroller External Interrupt 0 Status
76	HBPA	00	RW	High Byte of Microcontroller Program Memory Address
77	LBPA	00	RW	Low Byte of Microcontroller Program Memory Address
78	PWD	00	RW	Microcontroller Program Memory Write Data
79	PRD	–	R	Microcontroller Program Memory Read Data
7A	RSVD	XX	–	Reserved
7B	SSCS	13	RW	SCCB Speed Control SCCB Clock = XIN / 2 / (SCCS + 1)
7C	SCCC	07	RW	SCCB Command Bit[7]: Idle Bit[6]: Toggle SCS_ signal (reverse the current SCS_ signal) Bit[5]: Stop (perform SCCB stop condition) Bit[4]: Read bit (store data on SIO0 in SCCR[0] - see "SCCR" on page 16) Bit[3]: Read byte (store data on SIO0 in SCCR by MSB first - see "SCCR" on page 16) Bit[2]: Write bit (send SCCW[7] through SIO0 - see "SCCW" on page 16) Bit[1]: Write byte (send SCCW through SIO0 - see "SCCW" on page 16) Bit[0]: Start (perform SCCB start condition)
7D	SCCW	00	RW	SCCB Write Data
7E	SCCR	–	R	SCCB Read Data
7F	SCCB	–	R	SCCB Busy Bit[7]: Busy 0: Normal 1: Busy Bit[6:0]: Reserved
80	INT1M	FF	RW	Microcontroller External Interrupt Mask 1 Bit[7:2]: Reserved Bit[1]: SCCB ready Bit[0]: JPEG decoder header done

Table 6 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
81	INT1S	–	R	Microcontroller External Interrupt 1 Status
82	GPIO0R	–	R	GPIO0 Read Data
83	GPIO0D	FF	RW	GPIO0 Direction Control 0: Output 1: Input
84	GPIO0W	0F	RW	GPIO0 Write Data
85	GPIO1R	–	R	GPIO1 Read Data
86	GPIO1D	00	RW	GPIO1 Direction Control 0: Output 1: Input
87	GPIO1W	AA	RW	GPIO1 Write Data
88	JPHS	14	RW	JPEG Header Size
89	HJPES	–	R	High byte of JPEG Encoding Size (Real_Size/4)
8A	LJPES	–	R	Low byte of JPEG Encoding Size (Real_Size/4)
8B	JPQTA	00	RW	JPEG Quantization Table Address
8C	JPQTW	00	RW	JPEG Quantization Table Write Data
8D	JPSR	04	RW	JPEG Status Register Bit[7]: Byte stuff 0: Disabled 1: Enabled Bit[6]: Encoder table 0: Disabled 1: Enabled Bit[5]: Quantization table 0: Disabled 1: Enabled Bit[4]: Header 0: Disabled 1: Enabled Bit[3]: Decoder one shot 0: Disabled 1: Enabled Bit[2]: Encoder one shot 0: Disabled 1: Enabled Bit[1]: Operation modes 0: Encoding 1: Decoding Bit[0]: CODEC 0: Disabled 1: Enabled
8E	HBJEBC	1C	RW	High Byte of JPEG Encoder Block Count

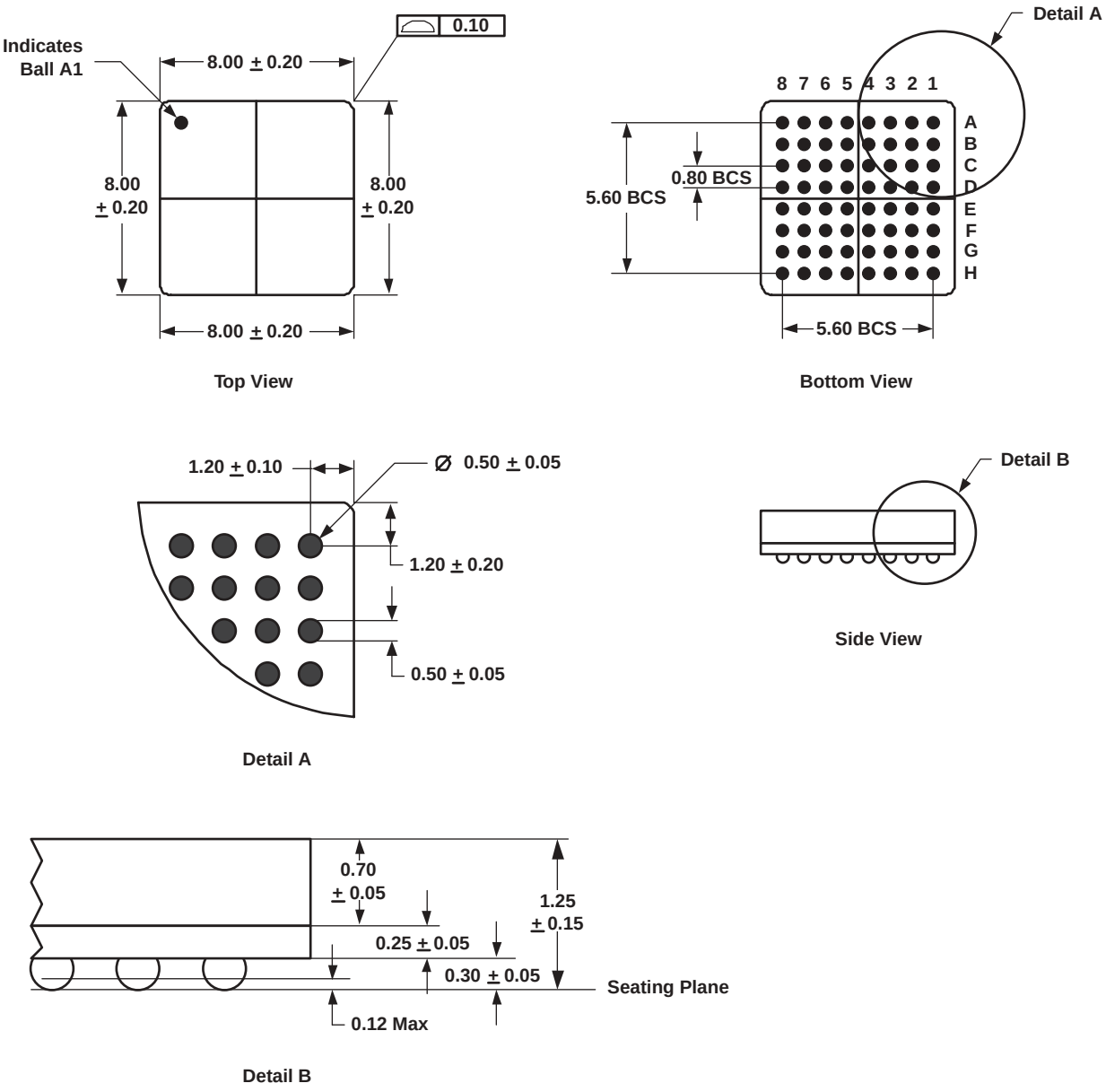
Table 6 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
8F	LBJEBC	20	RW	Low Byte of JPEG Encoder Block Count
90	STCS	–	R	Serial Bus Transmitting Checksum
91	SRCS	–	R	Serial Bus Receiving Checksum
92	JQTRD	–	R	JPEG Quantization Table Read Data
93	HBBRA	–	R	High Byte of Buffer Read Address
94	LBBRA	–	R	Low Byte of Buffer Read Address
95	SPC0	80	RW	Special Control Register 0 40h: 160 x 128 20h: 80 x 64 (for VGA) 3Ah: 80 x 64 (for CIF) 80h: Other
96	SPC1	00	RW	Special Control Register 1 00h: 160 x 128 00h: 80 x 64 (for VGA) 2Eh: 80 x 64 (for CIF) 80h: Other
97	SPC2	80	RW	Special Control Register 2 44h: 160 x 128 22h: 80 x 64 (for VGA) 38h: 80 x 64 (for CIF) 80h: Other
98	SPC3	00	RW	Special Control Register 3 44h: 160 x 128 22h: 80 x 64 (for VGA) E3h: 80 x 64 (for CIF) 00h: Other
99	SPC4	00	RW	Special Control Register 4 13h: 160 x 128 13h: 80 x 64 (for VGA) 13h: 80 x 64 (for CIF) 00h: Other
9A	SPC5	00	RW	Special Control Register 5 13h: 160 x 128 13h: 80 x 64 (for VGA) 13h: 80 x 64 (for CIF) 00h: Other
NOTE: All other registers are factory-reserved (DO NOT access).				

Package Specifications

The OV528-B64 uses a 64-pin BGA package. Refer to Figure 4 for package information.

Figure 4 OV528-B64 Package Specifications



NOTE: All dimensions are in mm

Note:

- *All information shown herein is current as of the revision and publication date. Please refer to the OmniVision web site (http://www.ovt.com) to obtain the current versions of all documentation.*

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