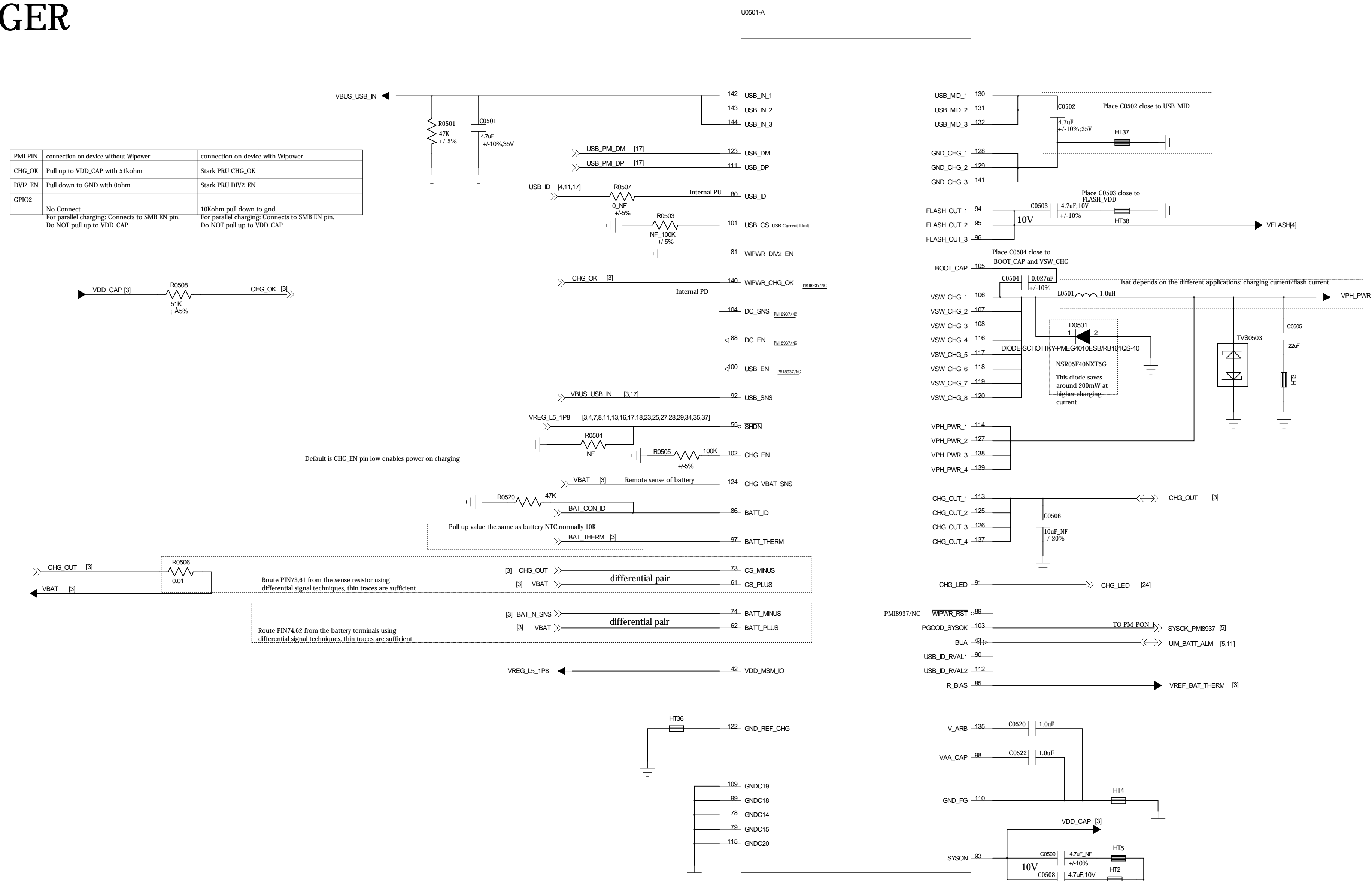
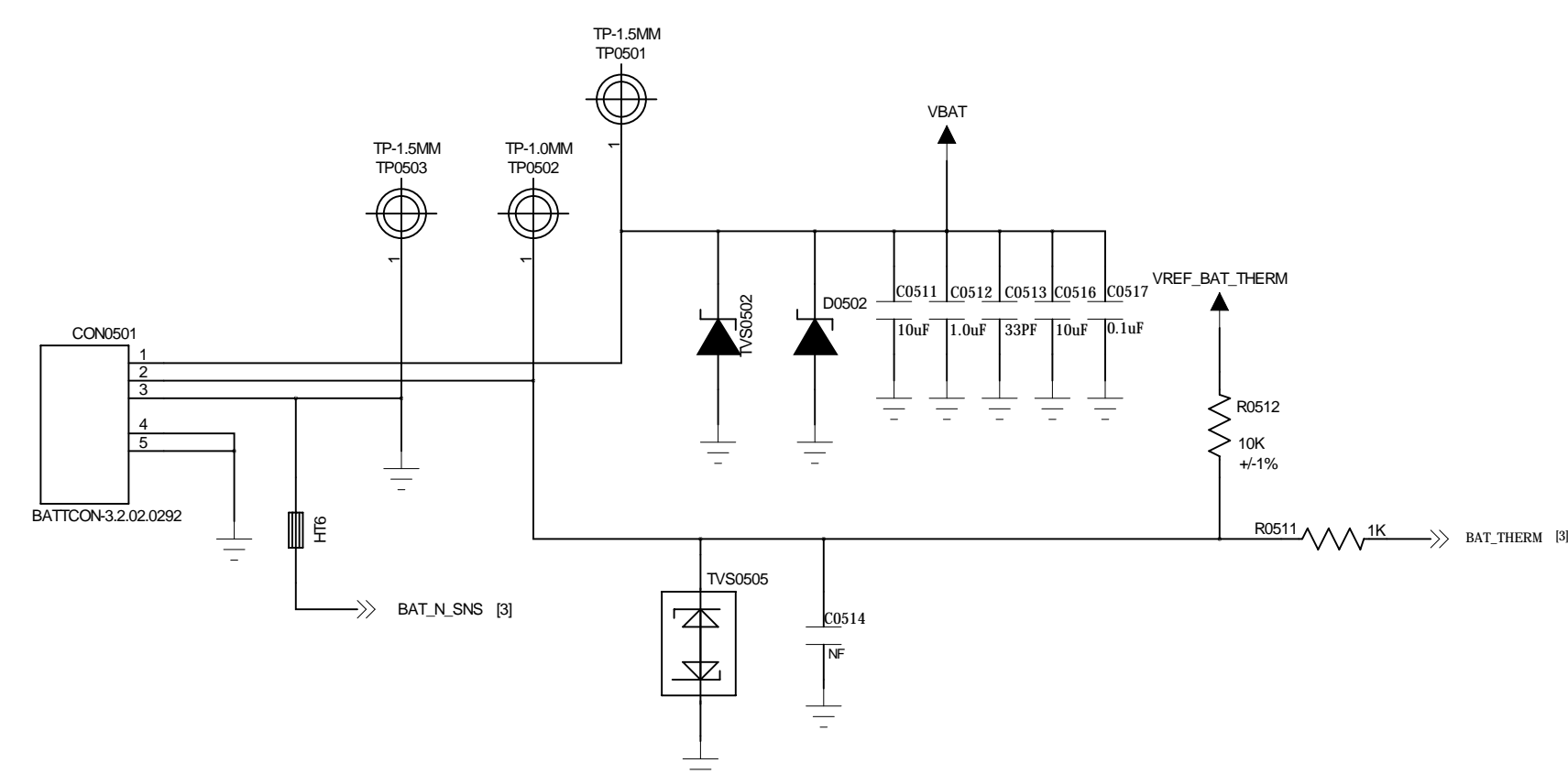


PMI8940 CHARGER

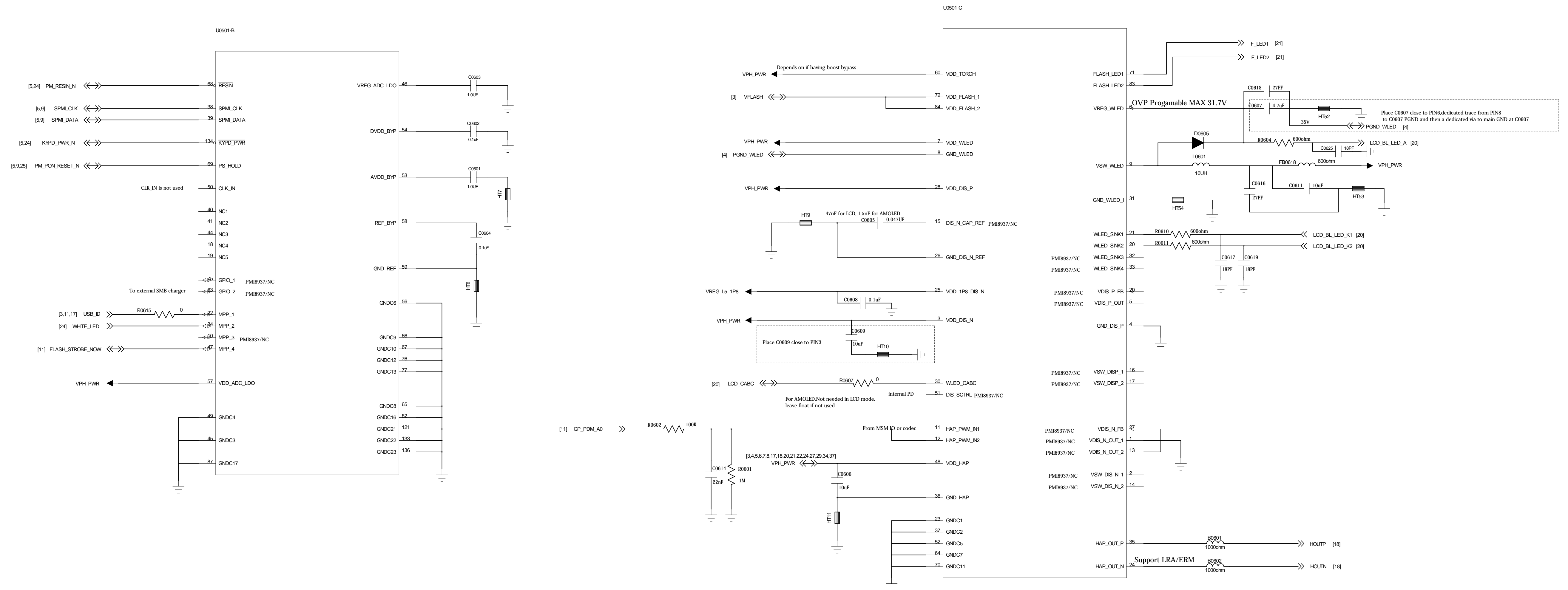


PMI_VDD_CAP net is 5VDC, cap is 0603.
Do not use 0402 as may derate to -80%.

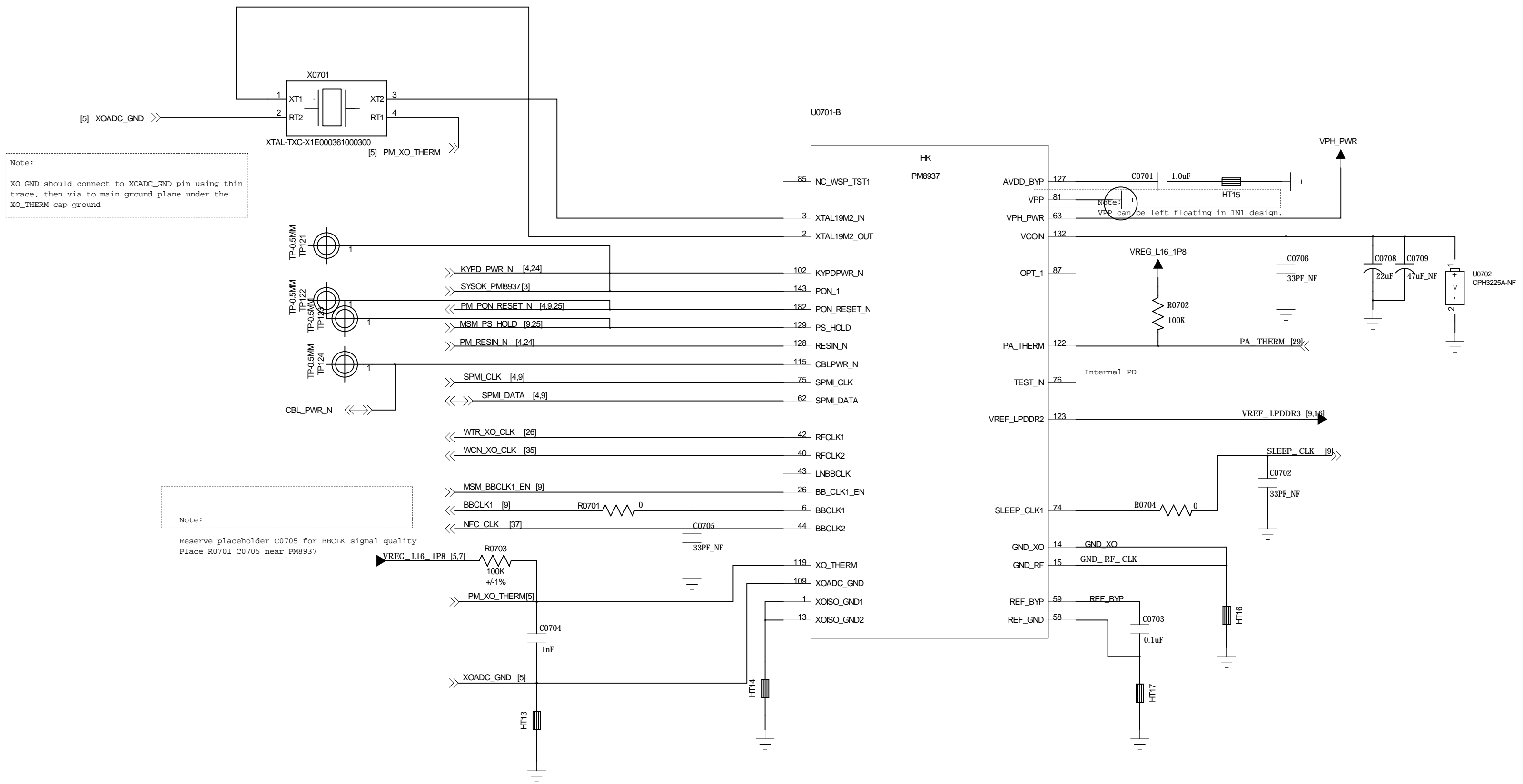
BATTERY CONNECTOR



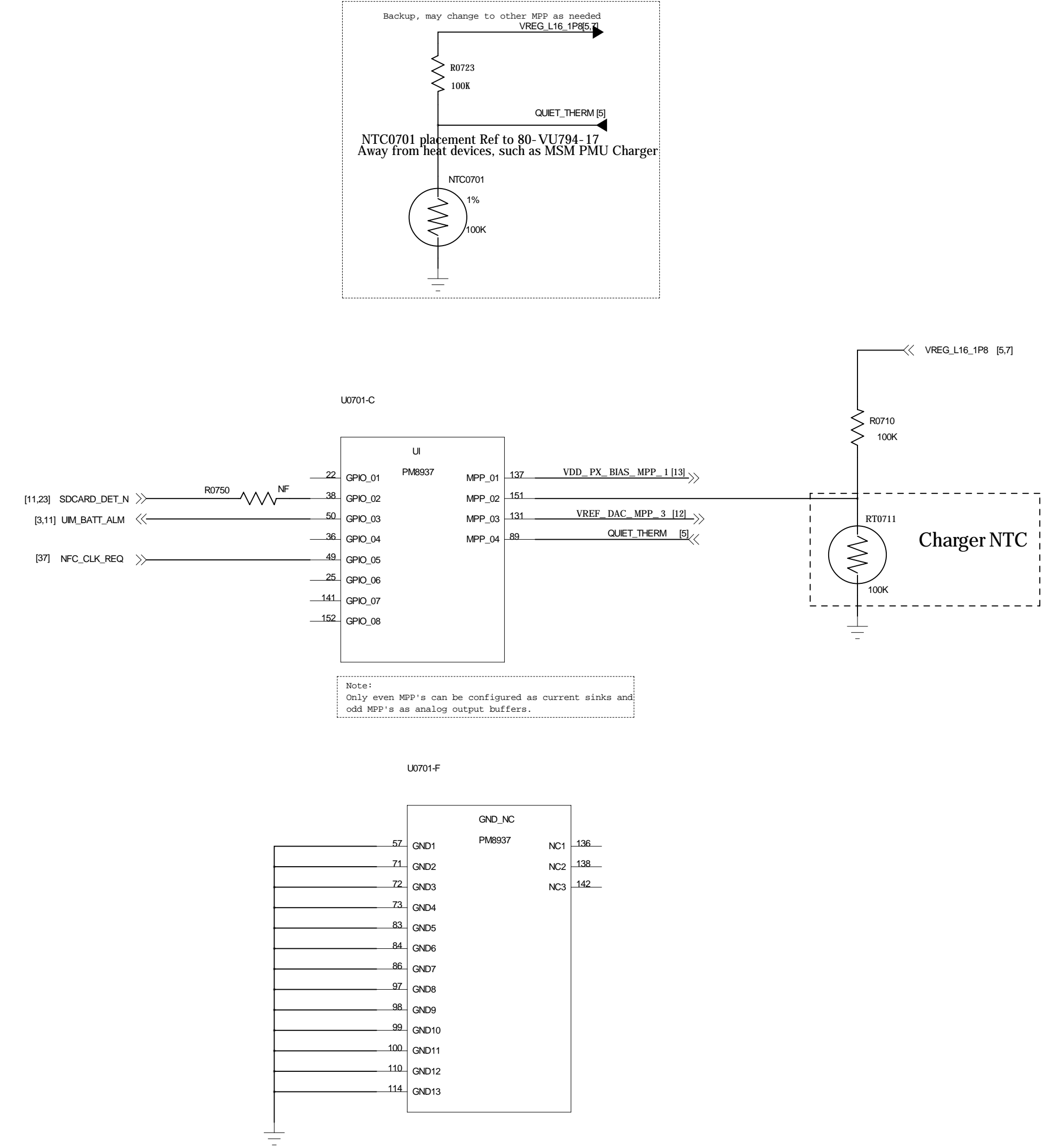
PMI8940 Control/Interface



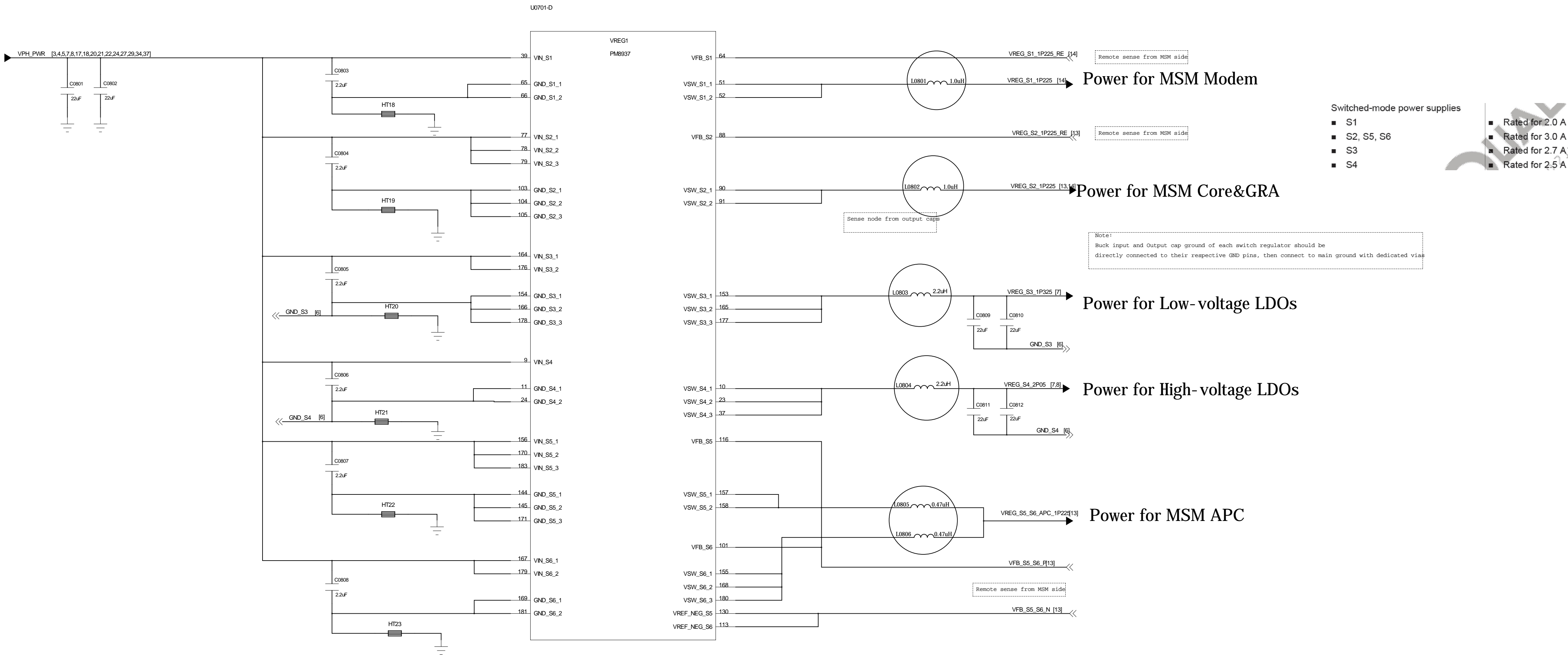
PM8937 Control



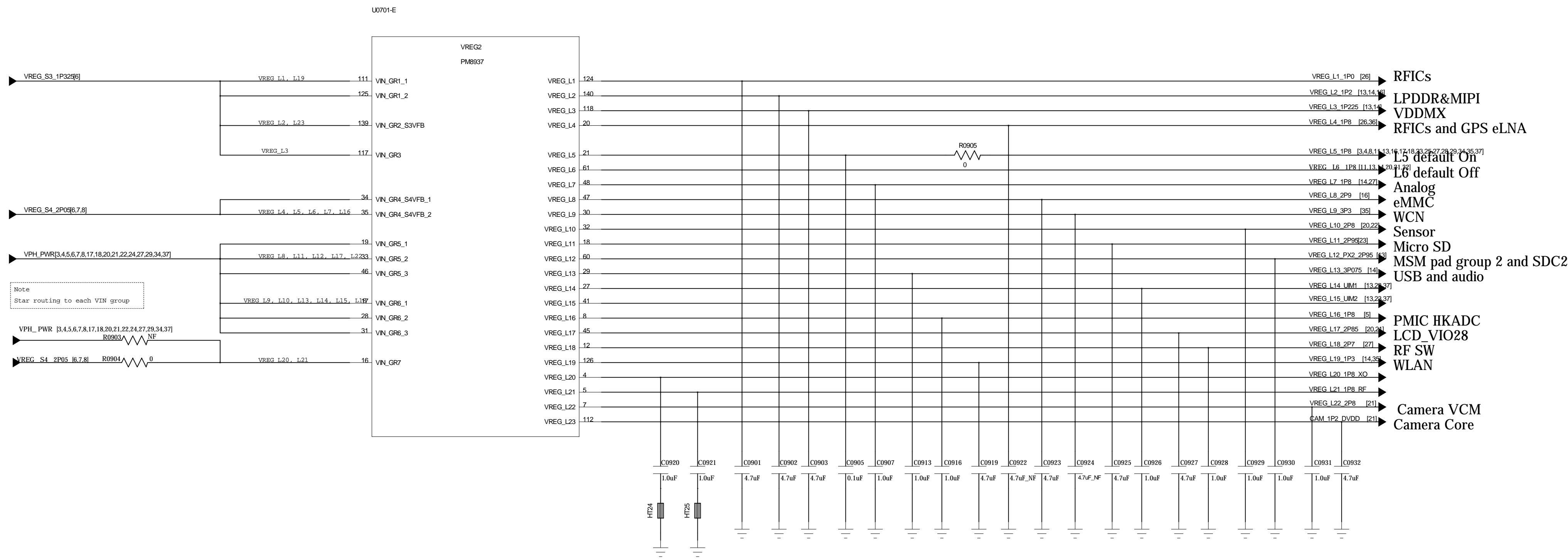
PM8937 MPPs



PM8937 BUCK CONVERTER



PM8937 LDO CIRCUITS



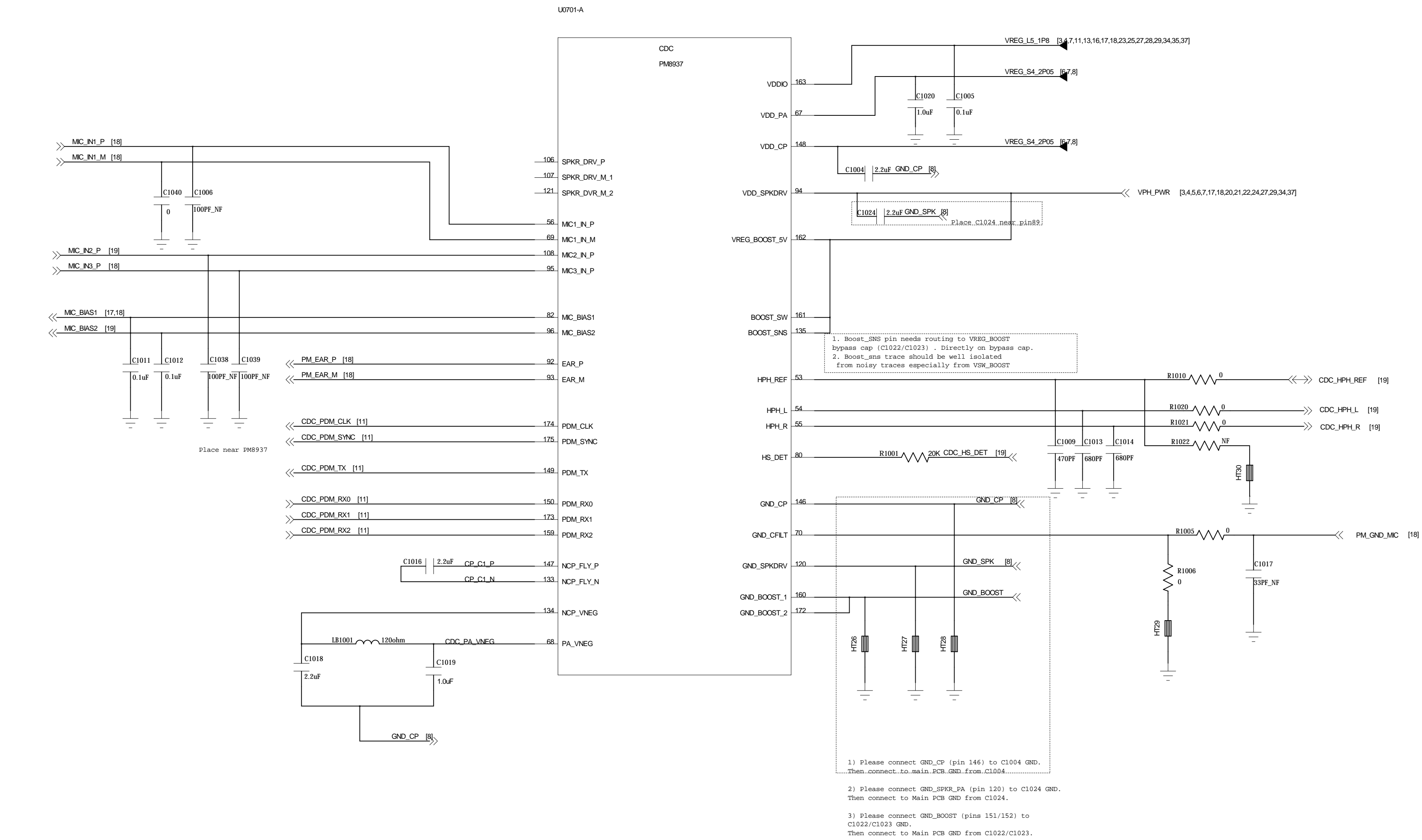
PSEUDO CAPLESS LDOs

L4*, L6, L8*, L9*, L10, L11*, L12, L14, L15, L17*, L18, L22, L23

L4*, L8*, L9*, L11*, L17*, still need validation as Pseudo-capless

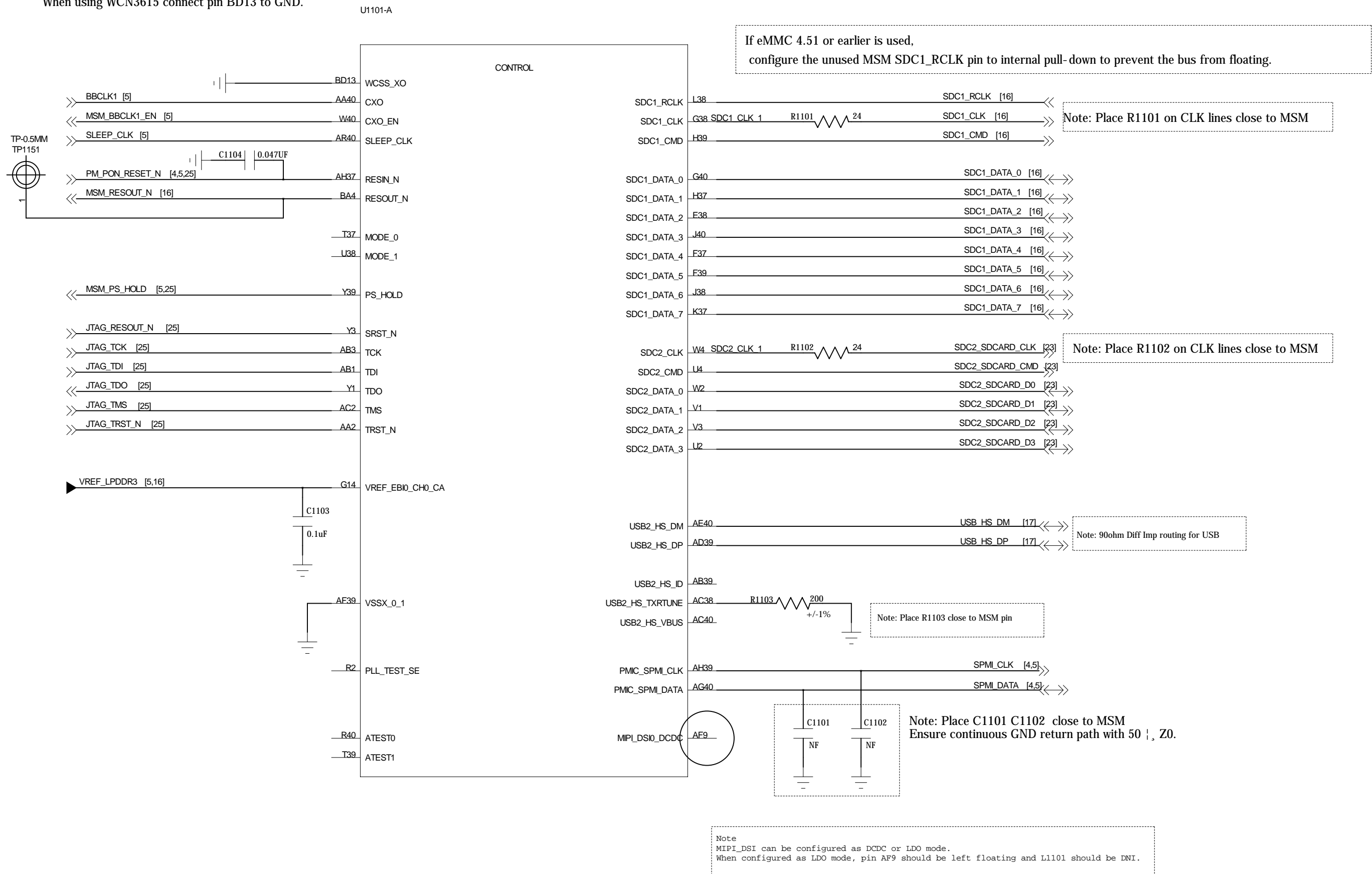
L5, L7, L13, L16 have internal PMIC Loads and require local CAPs.

PM8937 Codec

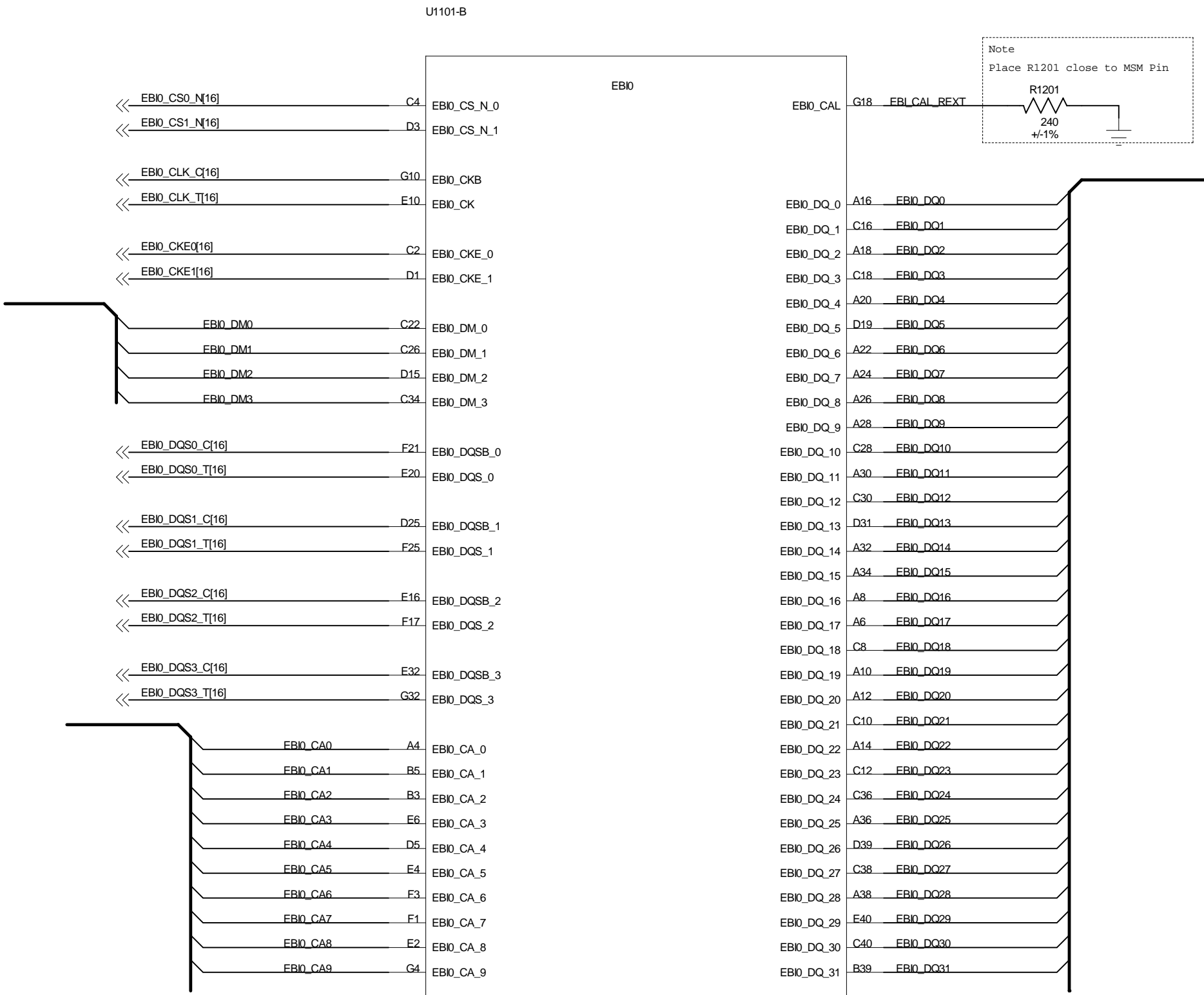


MSM8917 Control

Note: WCSS_XO signal required only for 5GHz.
When using WCN3615 connect pin BD13 to GND.



MSM8917 EBI



Title

Sheet

Date

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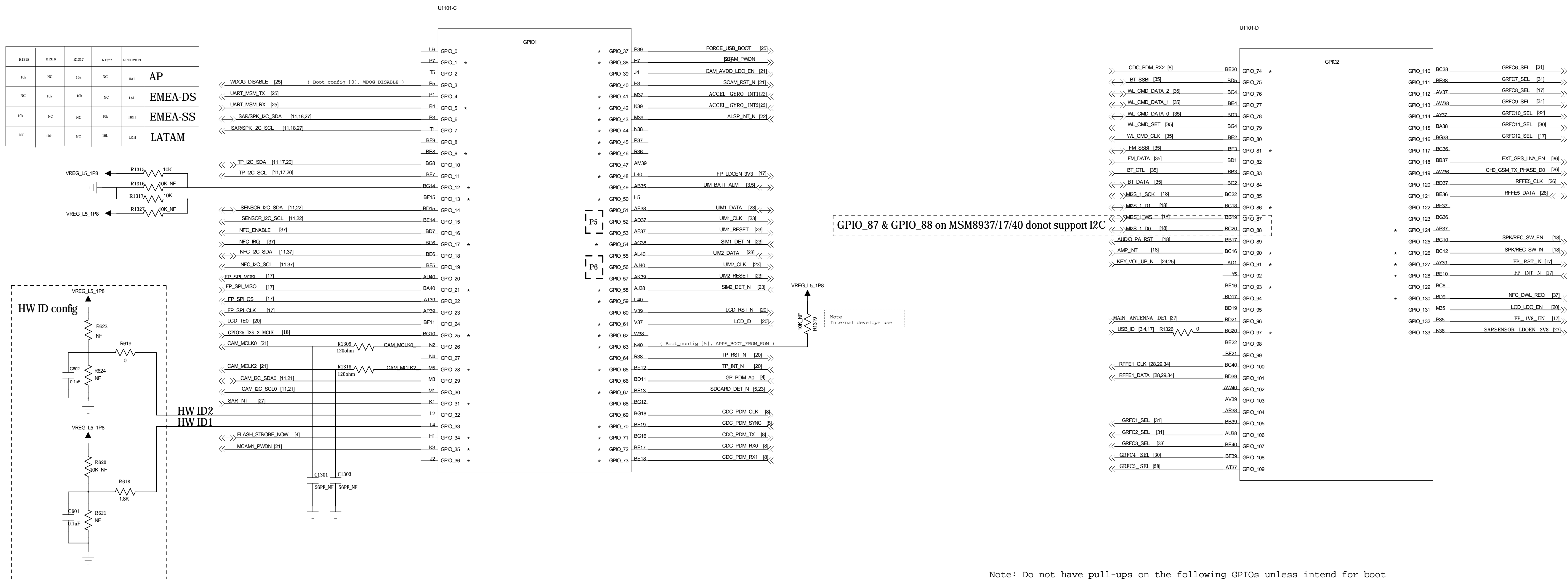
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Rev

MSM8917 GPIO

Note: Asterisks (*) indicate modem power management (MPM) wake-up pins

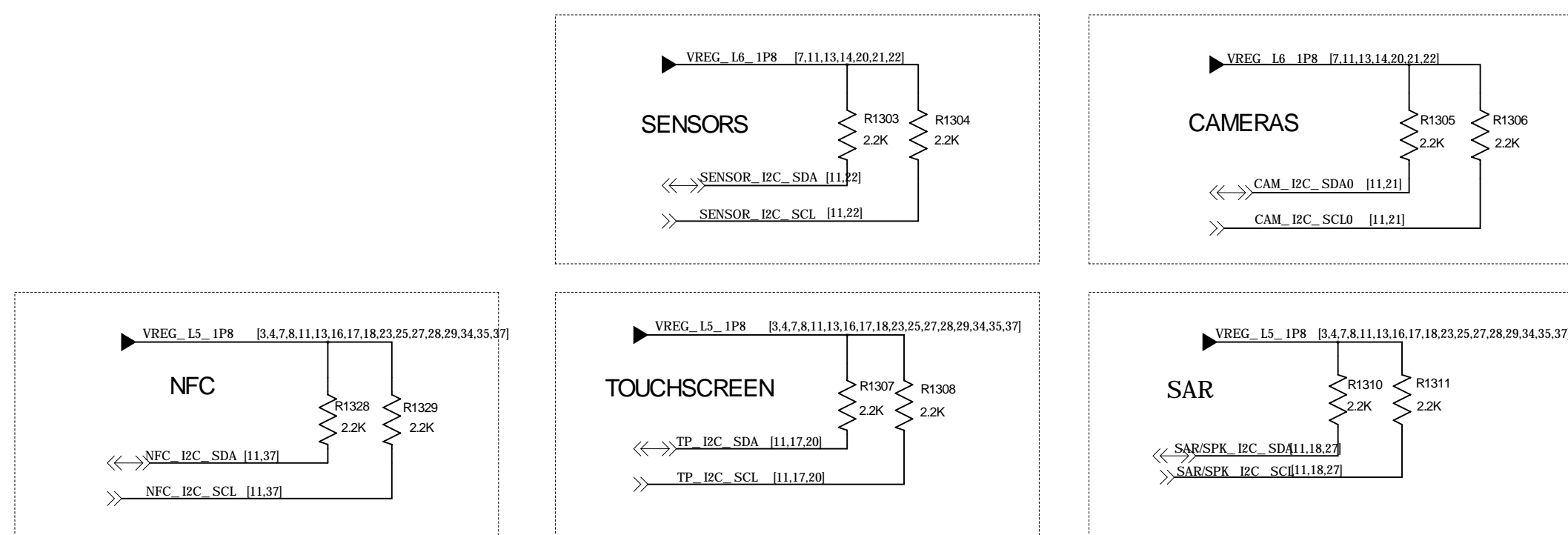


Note: Do not have pull-ups on the following GPIOs unless intend for boot or secure- boot related configurations:

GPIO_91, 107, 109

I2C PULL-UP RESISTORS

Note: Ensure SW sets these GPIOs (Sensor, CTP and Camera I2C bus) to inout pull down when the peripherals are powered off to eliminate leakage.

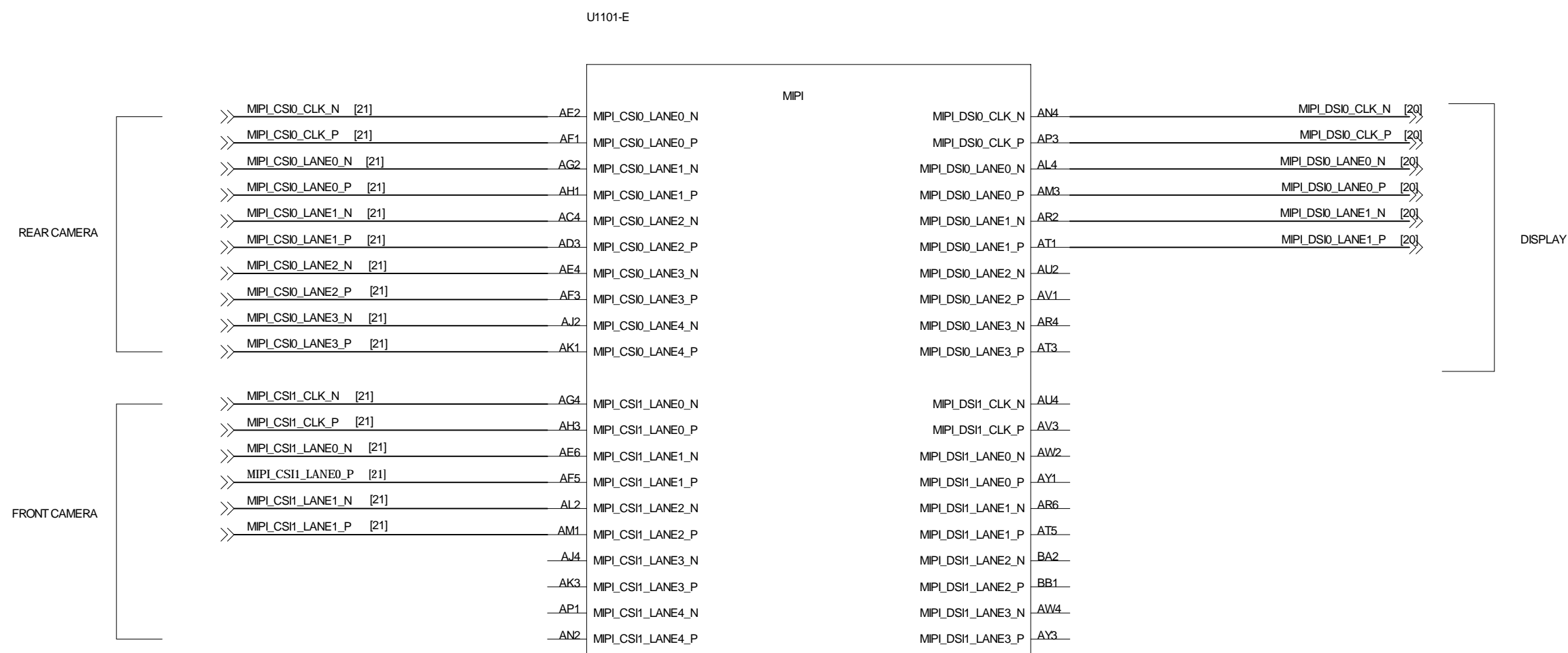


GPIO	BOOT_CONFIG
GPIO_3	BOOT_CONFIG[0]/WDOG_DISABLE
GPIO_111	BOOT_CONFIG[1]
GPIO_112	BOOT_CONFIG[2]
GPIO_88	BOOT_CONFIG[3]

BOOT_CONFIG[3:1]	BOOT_CONFIG
0b000	SDC1 -> SDC2 -> USB2.0
0b010	SDC1
0b100	SDC2-> SDC1

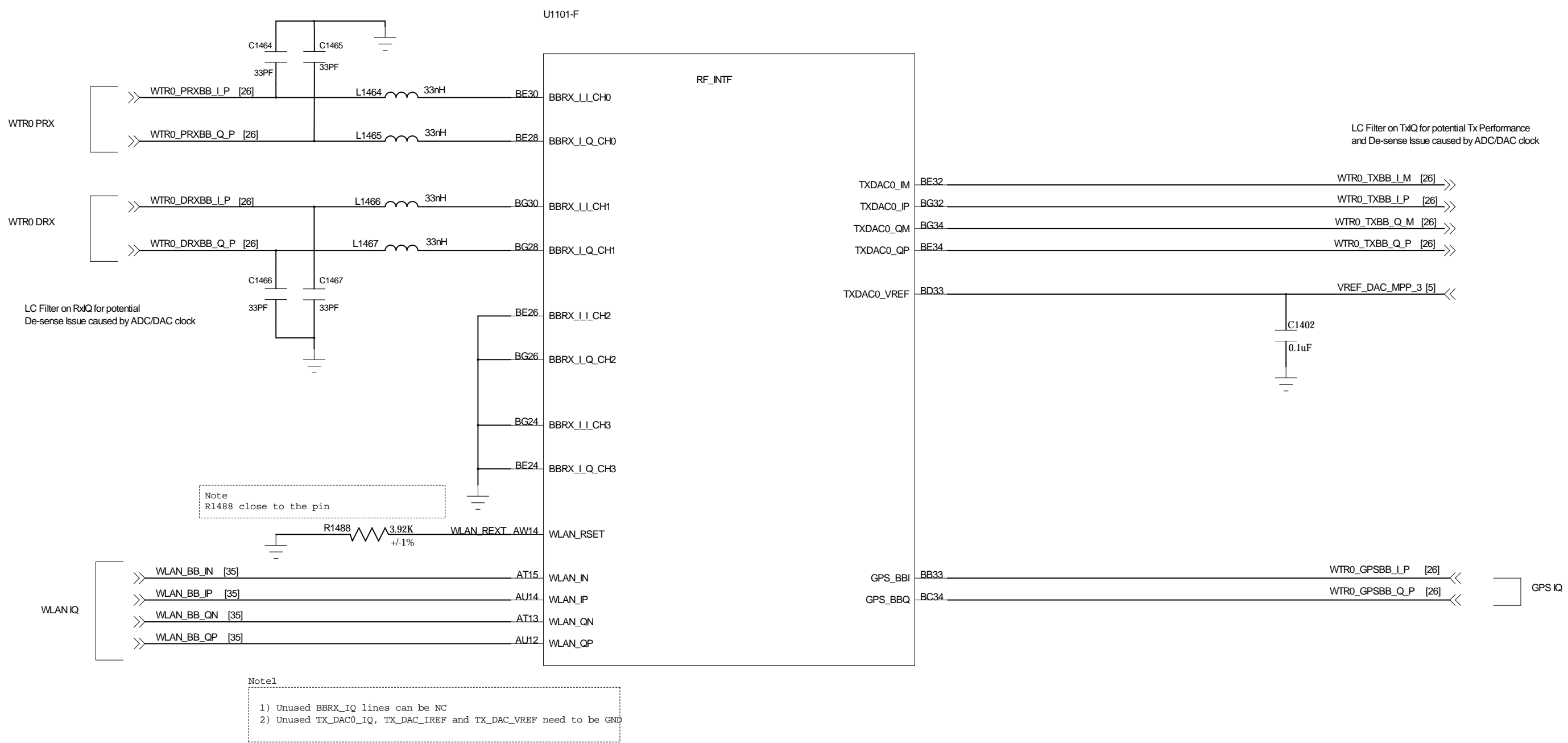
Default Boot Config (0b000) is SDCl(eMMC

MSM8917 MIPI

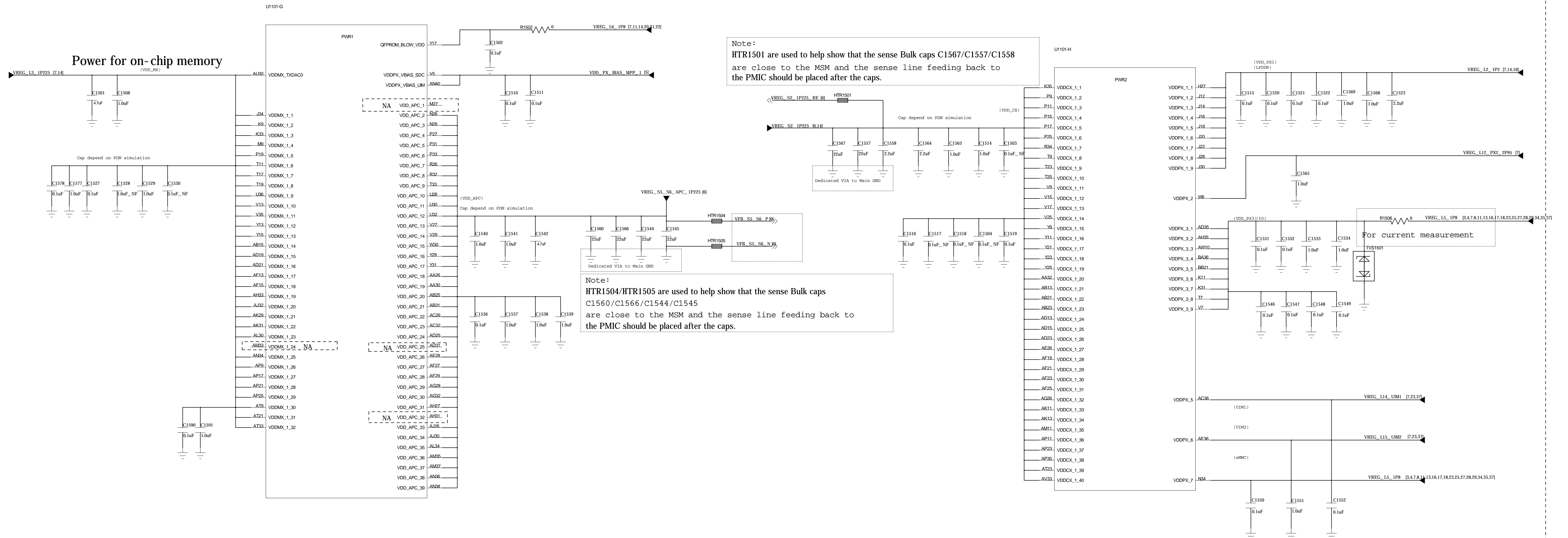


Note: If best EMI practices are followed for MIPI CSI/DSI signals, there is no need for common mode choke filters. You may choose to have placeholders for common mode depending upon your design constraints. Extreme care must be taken that no stubs are created by doing so.

MSM8917 RF Control

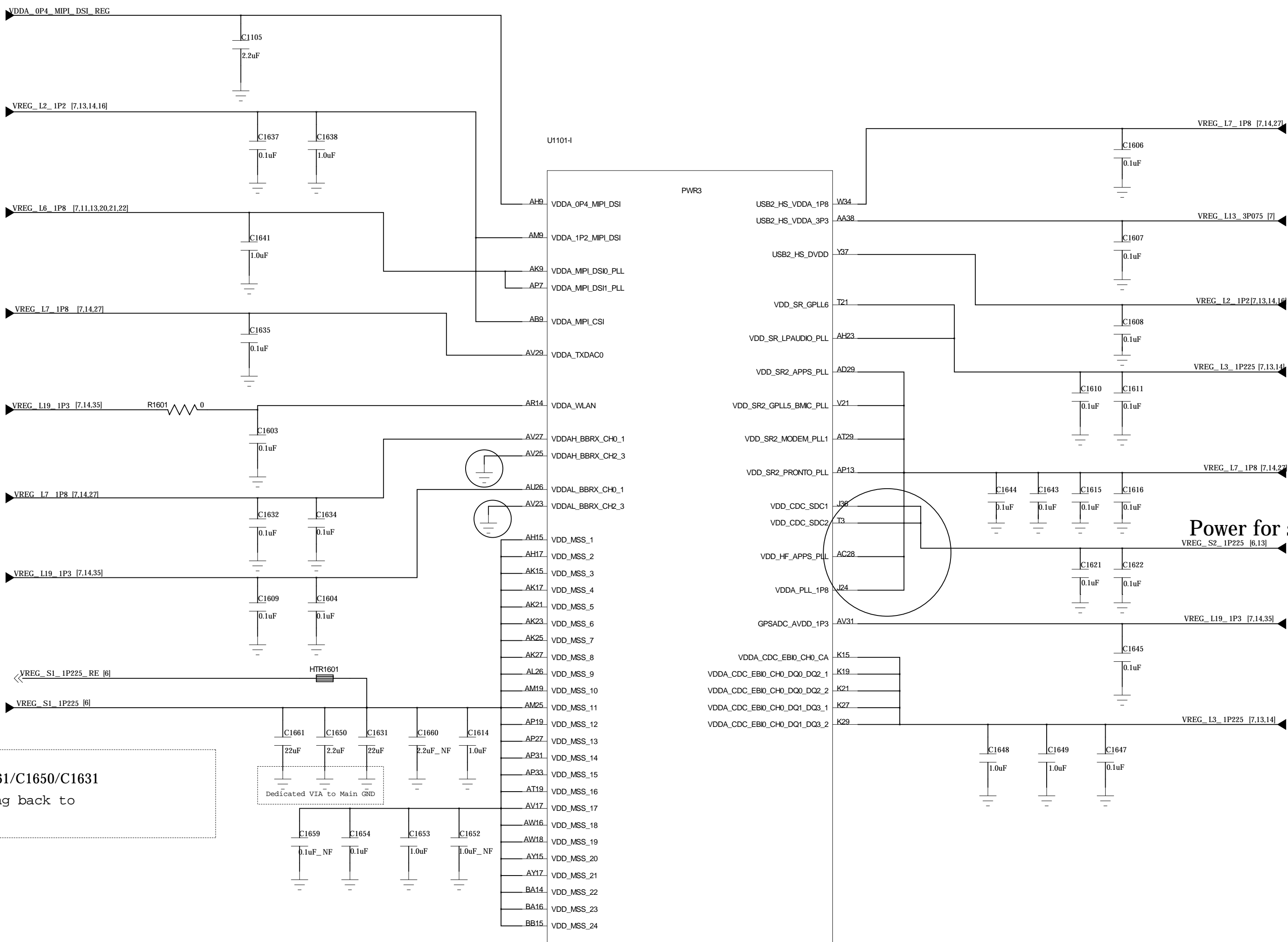


MSM8917 POWER1



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MSM8917 POWER2



Note:
HTR1601 are used to help show that the sense Bulk caps C1661/C1650/C1631 are close to the MSM and the sense line feeding back to the PMIC should be placed after the caps.

Power for secure digital calibration delay circuits

GND

U1101-L

GND3		
AB6	VSSX_0_154	VSSX_0_204
AB17	VSSX_0_155	VSSX_0_205
AB19	VSSX_0_156	VSSX_0_206
AB33	VSSX_0_157	VSSX_0_207
AC6	VSSX_0_158	VSSX_0_208
AC8	VSSX_0_159	VSSX_0_209
AD6	VSSX_0_160	VSSX_0_210
AD17	VSSX_0_161	VSSX_0_211
AD33	VSSX_0_162	NA
AE30	VSSX_0_163	VSSX_0_213
AE32	VSSX_0_164	NA
AF17	VSSX_0_165	VSSX_0_215
AF31	VSSX_0_166	VSSX_0_216
AF33	VSSX_0_167	VSSX_0_217
AG30	VSSX_0_168	VSSX_0_218
AH6	VSSX_0_169	VSSX_0_219
AH11	VSSX_0_170	VSSX_0_220
AH13	VSSX_0_171	VSSX_0_221
AH19	VSSX_0_172	VSSX_0_222
AH25	VSSX_0_173	VSSX_0_223
AH29	VSSX_0_174	VSSX_0_224
AL28	VSSX_0_175	VSSX_0_225
AL34	VSSX_0_176	VSSX_0_226
AL36	VSSX_0_177	VSSX_0_227
AK19	VSSX_0_178	VSSX_0_228
AK33	VSSX_0_179	VSSX_0_229
AK35	VSSX_0_180	VSSX_0_230
AK37	VSSX_0_181	VSSX_0_231
AL28	VSSX_0_182	VSSX_0_232
AL36	VSSX_0_183	VSSX_0_233
AL38	VSSX_0_184	VSSX_0_234
AM15	VSSX_0_185	VSSX_0_235
AM17	VSSX_0_186	VSSX_0_236
AM21	VSSX_0_187	VSSX_0_237
AM23	VSSX_0_188	BG40
AM27	VSSX_0_189	
AM29	VSSX_0_190	
AP15	VSSX_0_191	
AT7	VSSX_0_192	
AT25	VSSX_0_193	
AT35	VSSX_0_194	
AL6	VSSX_0_195	
AL32	VSSX_0_196	
AV5	VSSX_0_197	
AV7	VSSX_0_198	
AV9	VSSX_0_199	
AV11	VSSX_0_200	
AV19	VSSX_0_201	
AV21	VSSX_0_202	
AV35	VSSX_0_203	

U1101-J

GND1		
AK2	VSSX_0_2	VSSX_0_32
AN8	VSSX_0_3	VSSX_0_33
AH7	VSSX_0_4	VSSX_0_34
AK3	VSSX_0_5	VSSX_0_35
AM6	VSSX_0_6	
AM7	VSSX_0_7	
AP5	VSSX_0_8	
		VSSX_0_36
		VSSX_0_37
		VSSX_0_38
AW30	VSSX_0_9	VSSX_0_38
AY29	VSSX_0_10	VSSX_0_38
BD3	VSSX_0_11	
BC32	VSSX_0_12	VSSX_0_40
BD31	VSSX_0_13	VSSX_0_41
BF31	VSSX_0_14	
BF33	VSSX_0_15	VSSX_0_42
BF35	VSSX_0_16	VSSX_0_43
		VSSX_0_44
AV13	VSSX_0_17	VSSX_0_45
		VSSX_0_46
AW28	VSSX_0_18	VSSX_0_47
AY27	VSSX_0_19	
BC28	VSSX_0_20	
BC34	VSSX_0_21	VSSX_0_48
BD27	VSSX_0_22	VSSX_0_49
BD29	VSSX_0_23	
BE27	VSSX_0_24	
BF29	VSSX_0_25	VSSX_0_50
AY25	VSSX_0_26	
BC24	VSSX_0_27	
BC26	VSSX_0_28	
BD25	VSSX_0_29	
BF25	VSSX_0_30	
		VSSX_0_51
AT27	VSSX_0_31	VSSX_0_52
		VSSX_0_53

U1101-K

GND2		
A2	VSSX_0_54	VSSX_0_104
A40	VSSX_0_55	VSSX_0_105
B1	VSSX_0_56	VSSX_0_106
B7	VSSX_0_57	VSSX_0_107
B9	VSSX_0_58	VSSX_0_108
B11	VSSX_0_59	VSSX_0_109
B13	VSSX_0_60	VSSX_0_110
B15	VSSX_0_61	VSSX_0_111
B17	VSSX_0_62	VSSX_0_112
B19	VSSX_0_63	VSSX_0_113
B21	VSSX_0_64	VSSX_0_114
B23	VSSX_0_65	VSSX_0_115
B25	VSSX_0_66	VSSX_0_116
B27	VSSX_0_67	VSSX_0_117
B29	VSSX_0_68	VSSX_0_118
B31	VSSX_0_69	VSSX_0_119
B33	VSSX_0_70	VSSX_0_120
B35	VSSX_0_71	VSSX_0_121
B37	VSSX_0_72	VSSX_0_122
C6	VSSX_0_73	NA
C14	VSSX_0_74	VSSX_0_123
C20	VSSX_0_75	VSSX_0_125
C24	VSSX_0_76	VSSX_0_126
C32	VSSX_0_77	VSSX_0_127
D7	VSSX_0_78	VSSX_0_128
D9	VSSX_0_79	VSSX_0_129
D11	VSSX_0_80	VSSX_0_130
D13	VSSX_0_81	VSSX_0_131
D17	VSSX_0_82	VSSX_0_132
D21	VSSX_0_83	VSSX_0_133
D23	VSSX_0_84	VSSX_0_134
D27	VSSX_0_85	VSSX_0_135
D29	VSSX_0_86	VSSX_0_136
D33	VSSX_0_87	VSSX_0_137
D35	VSSX_0_88	VSSX_0_138
D37	VSSX_0_89	VSSX_0_139
E8	VSSX_0_90	VSSX_0_140
E18	VSSX_0_91	VSSX_0_141
E22	VSSX_0_92	VSSX_0_142
E24	VSSX_0_93	VSSX_0_143
E26	VSSX_0_94	VSSX_0_144
E28	VSSX_0_95	VSSX_0_145
E30	VSSX_0_96	VSSX_0_146
E34	VSSX_0_97	VSSX_0_147
E36	VSSX_0_98	VSSX_0_148
F7	VSSX_0_99	VSSX_0_149
F13	VSSX_0_100	VSSX_0_150
F23	VSSX_0_101	VSSX_0_151
G2	VSSX_0_102	VSSX_0_152
G6	VSSX_0_103	VSSX_0_153

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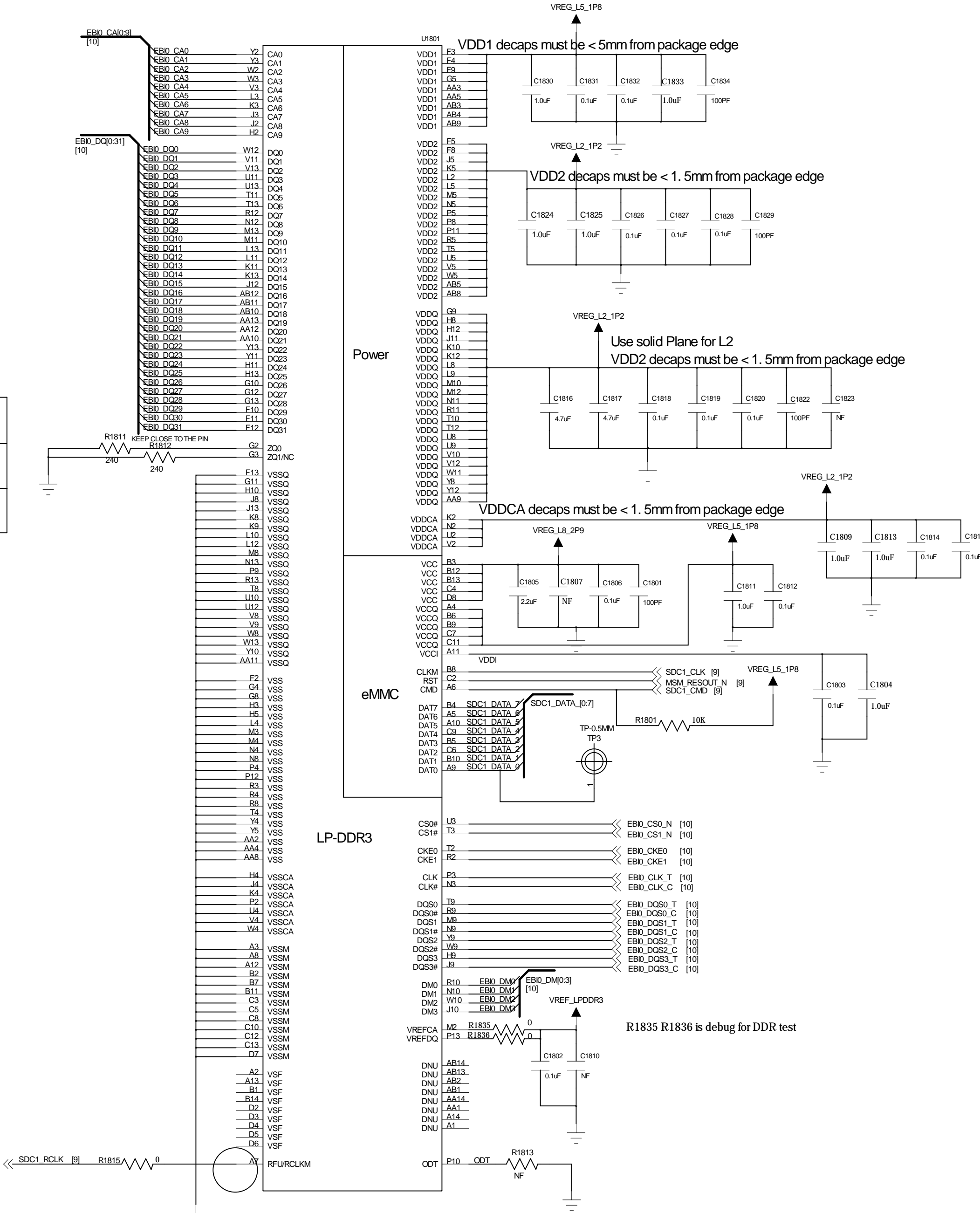
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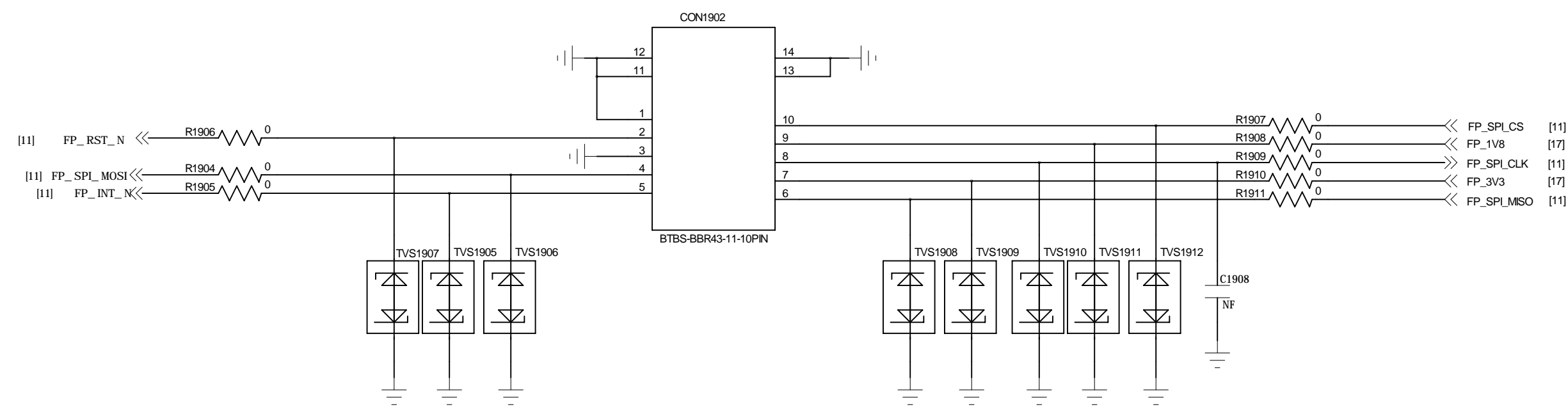
MEMORY:LPDDR3+EMMC

	MICRO/HYNIX	SAMSUNG
U1501.G3	ZQ1	NC
U1501.A7	RFU	RCLK

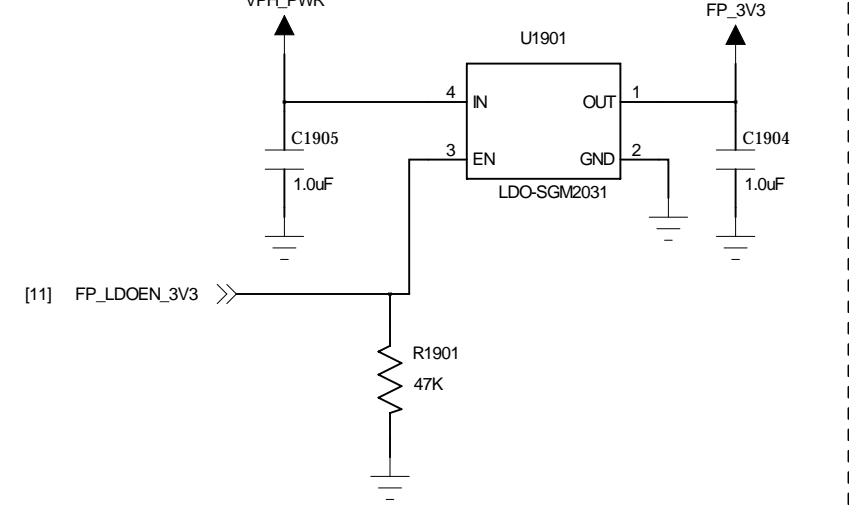


Note: Pull-up resistors on SDC1_DATA are PCB and eMMC vender dependent

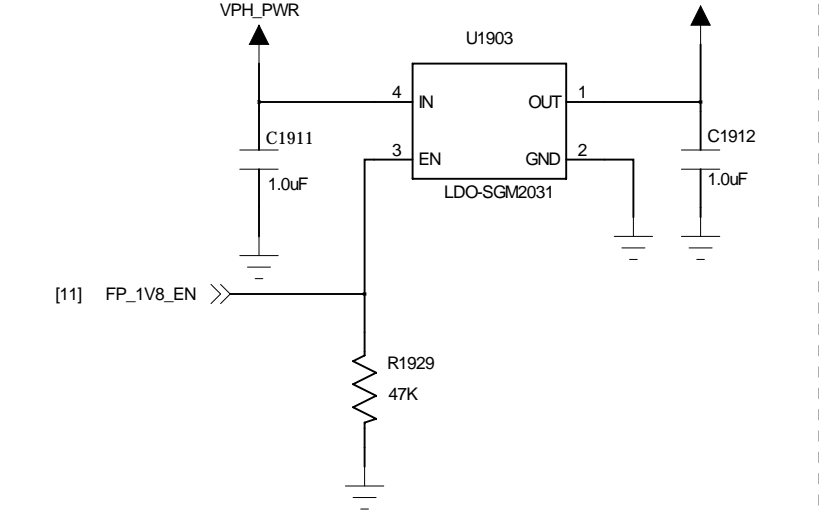
FingerPrint



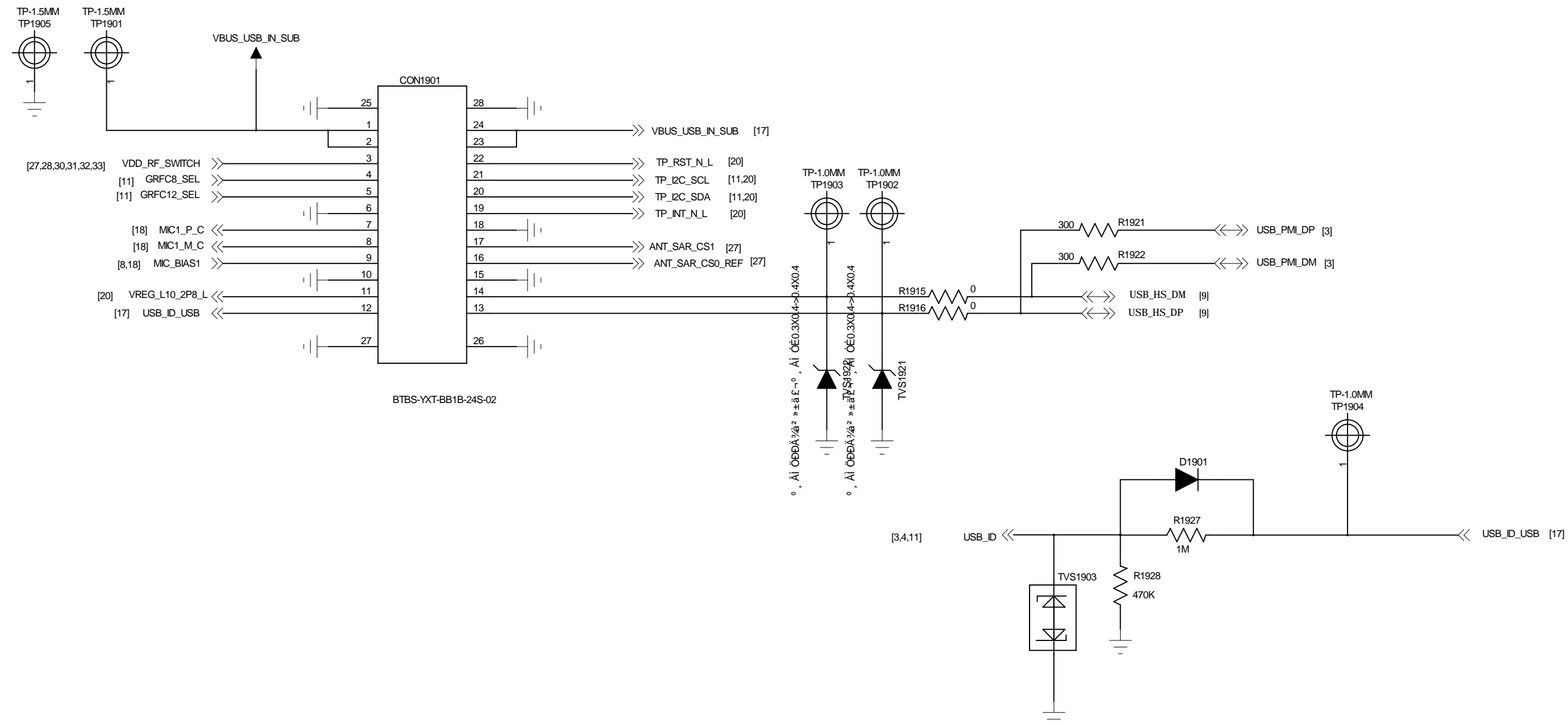
LDO-3.3V



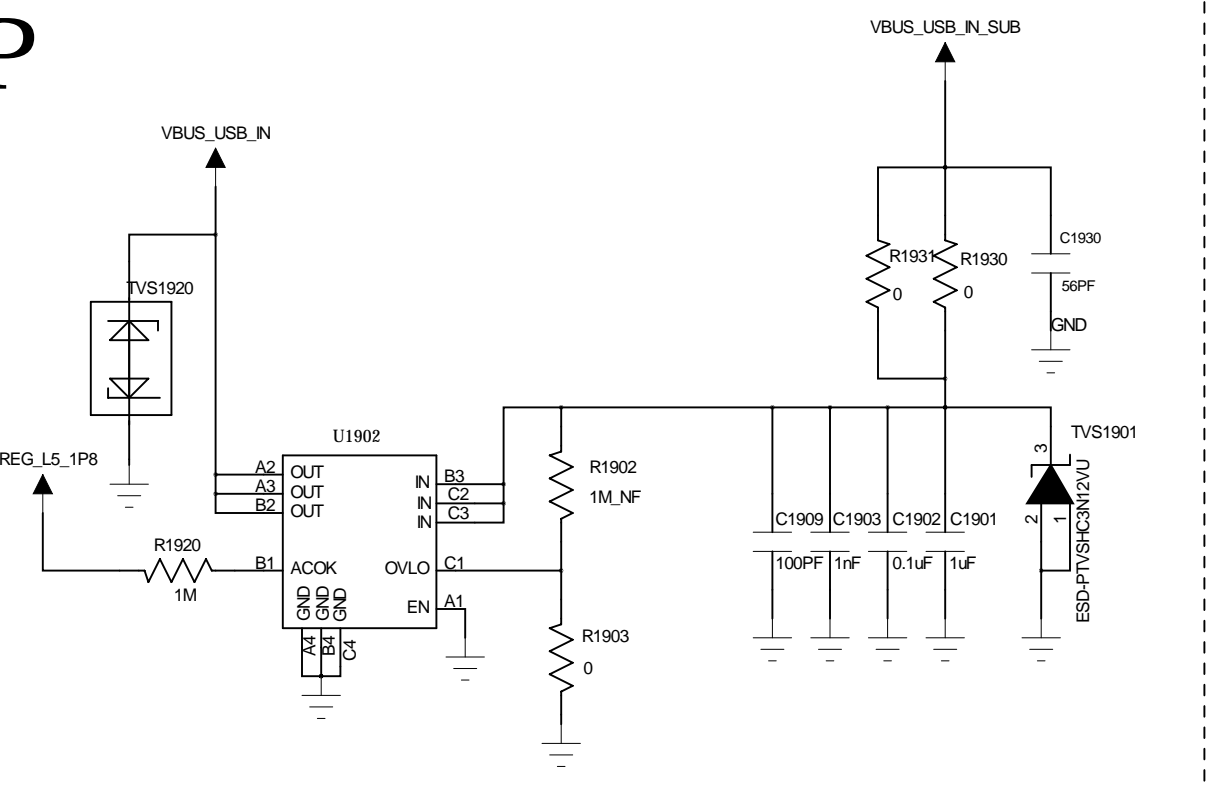
LDO-1.8V



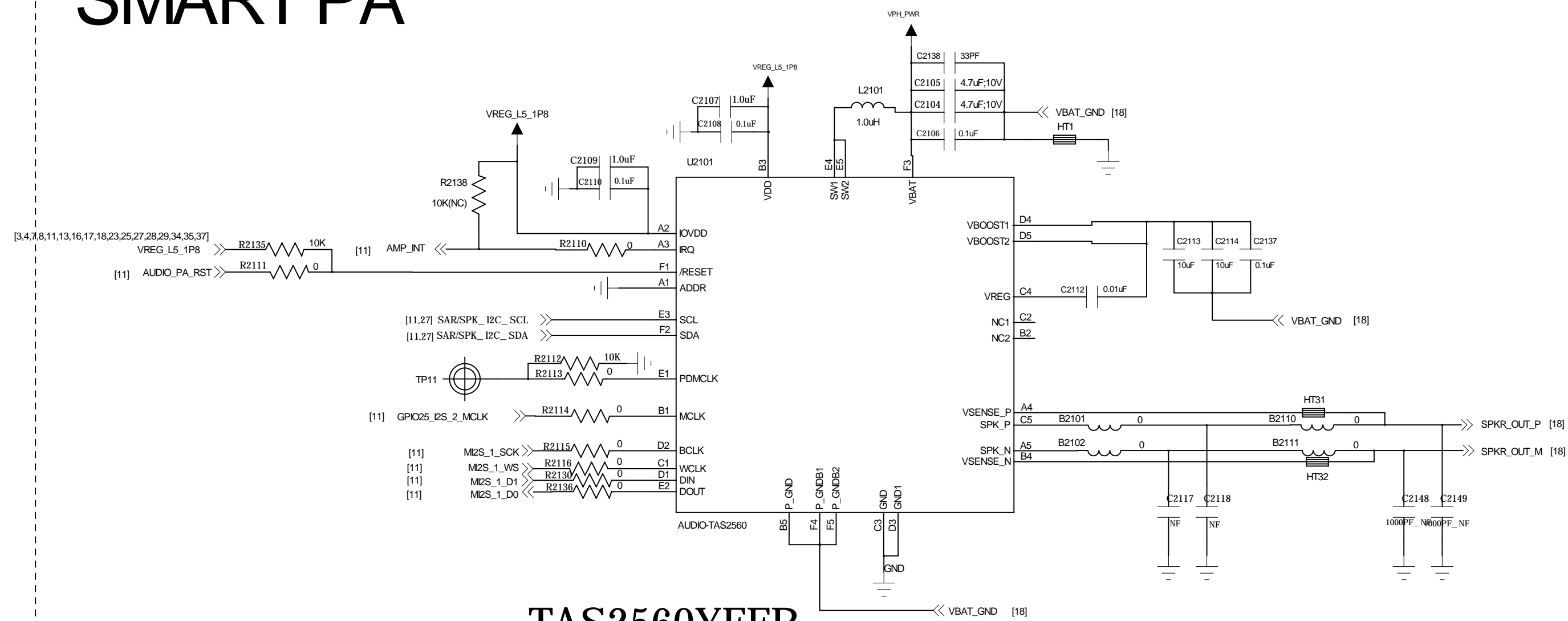
SUB_CONNECTOR



OVP

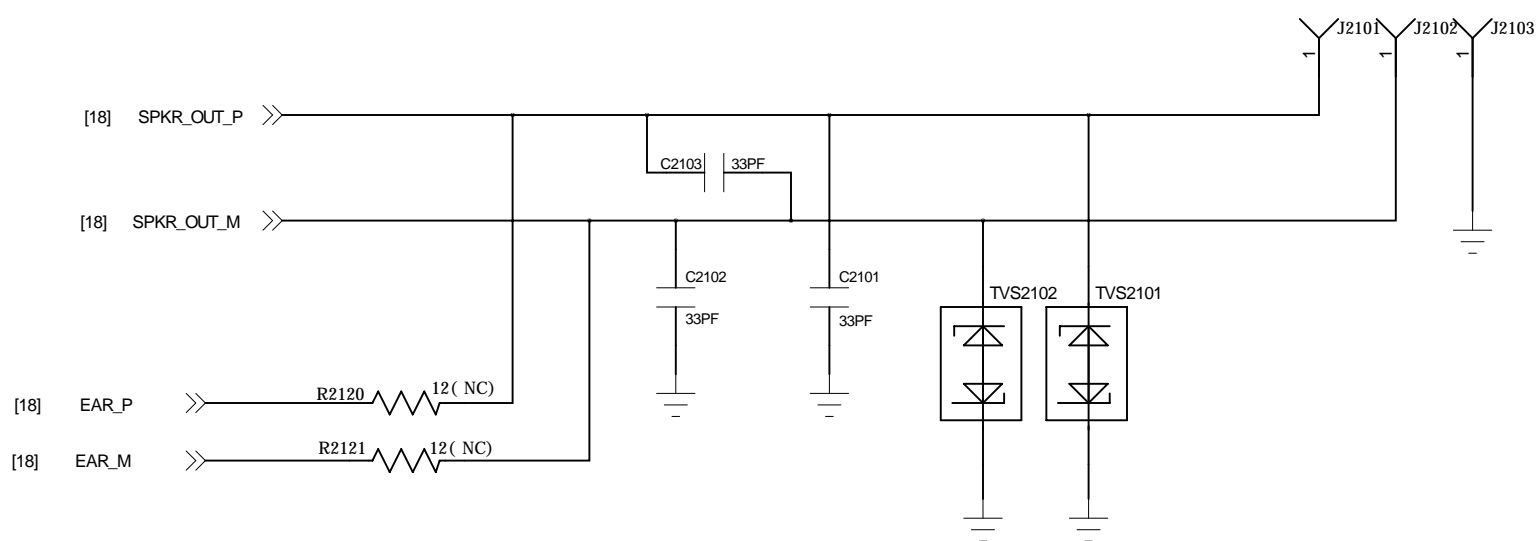


SMART PA

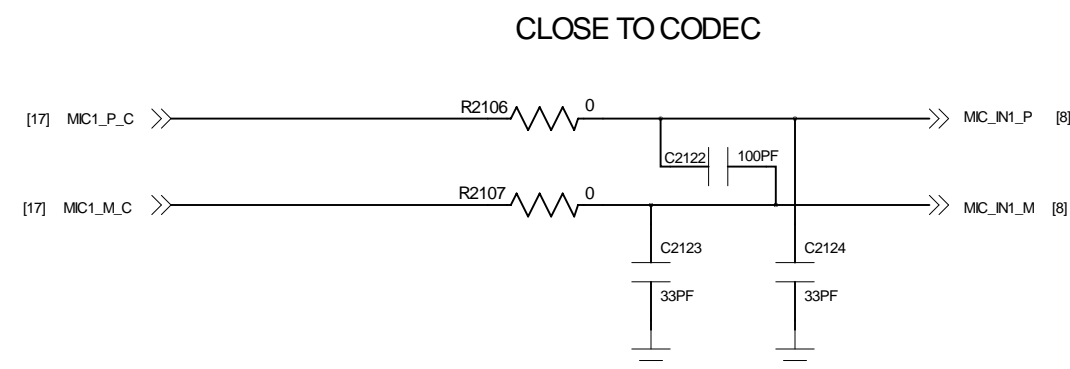


TAS2560YFFR

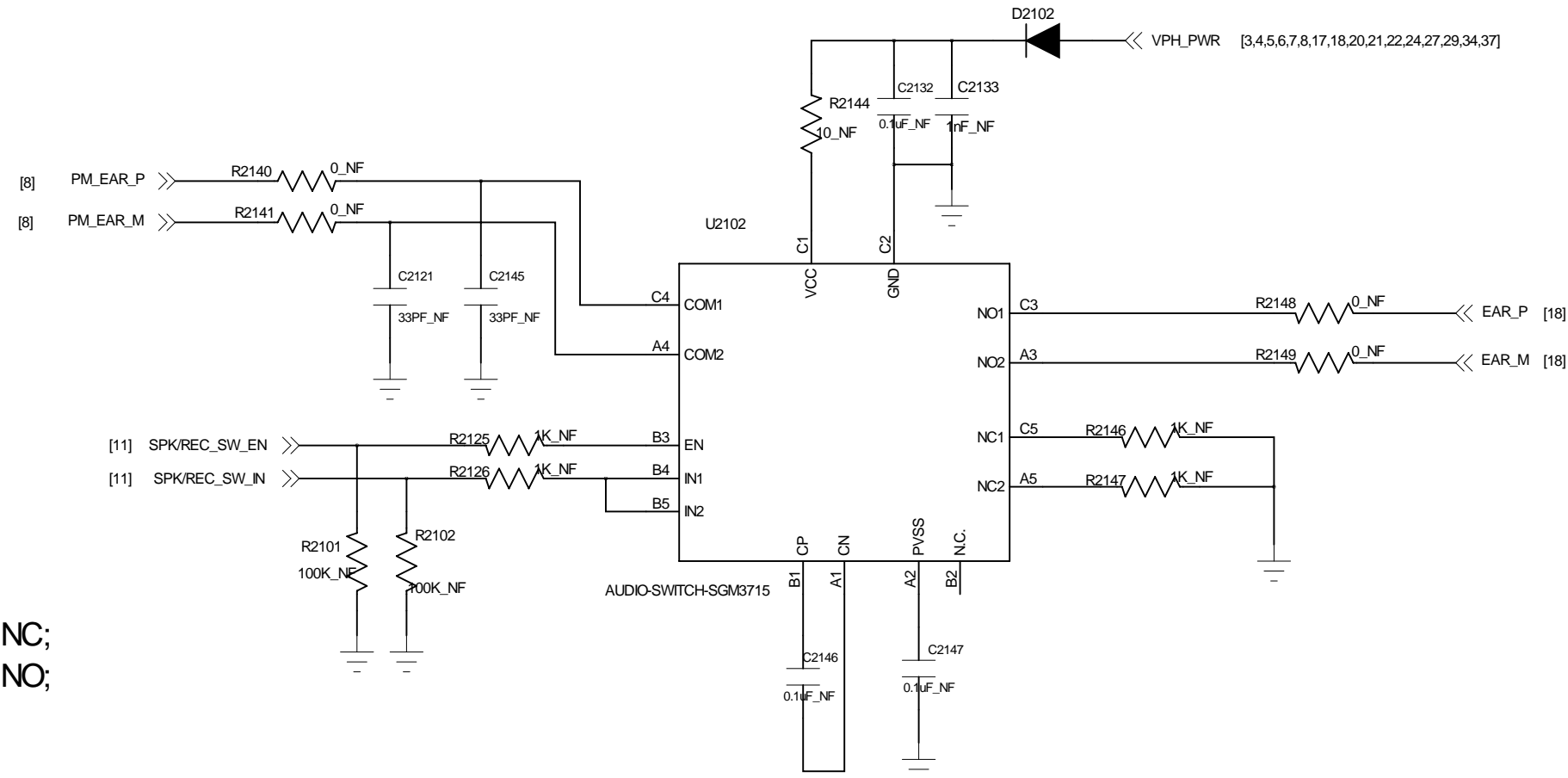
REC&SPK



PRIMARY MIC

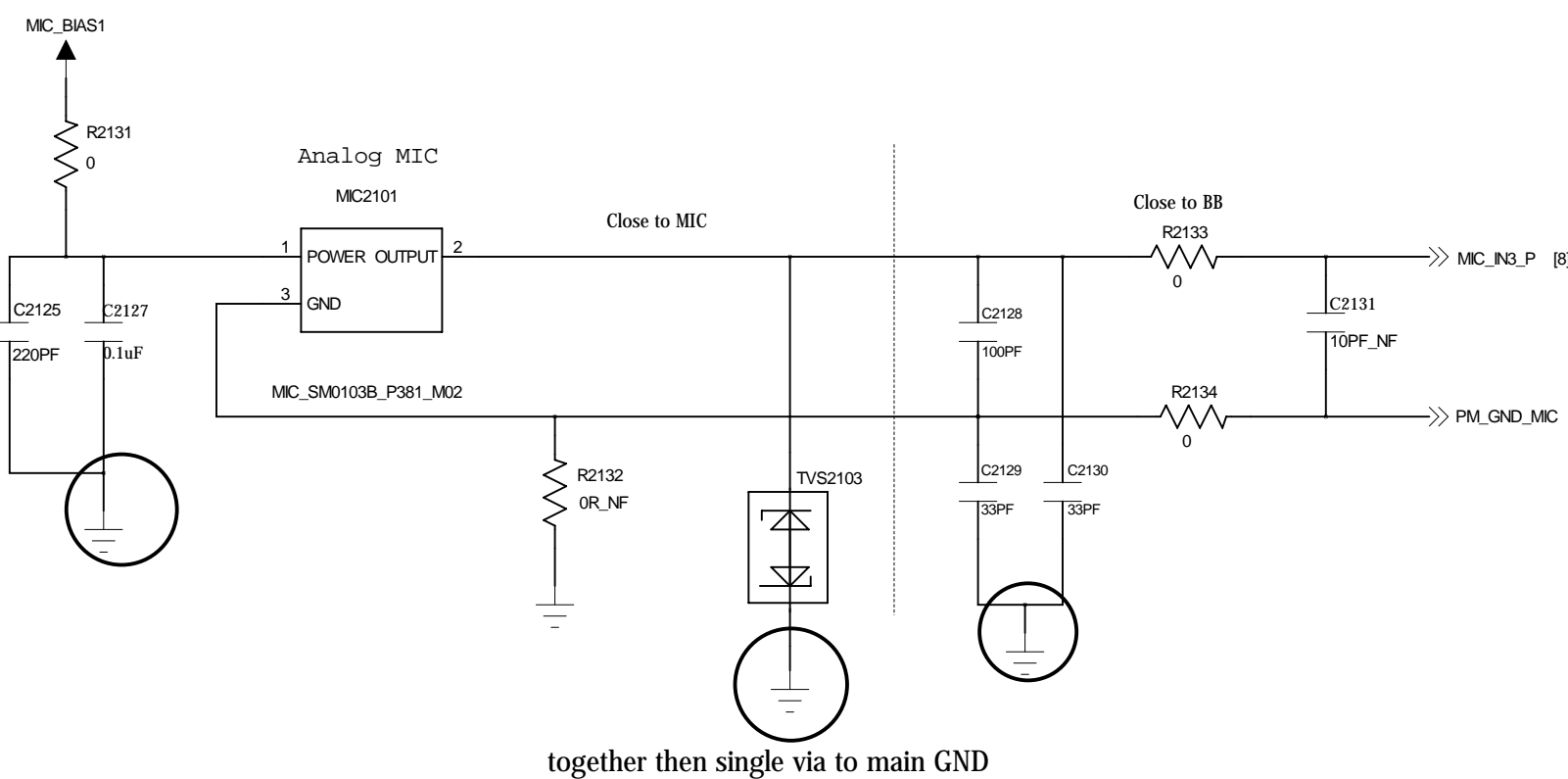


SWITCH-ANOLOG-SGM3715



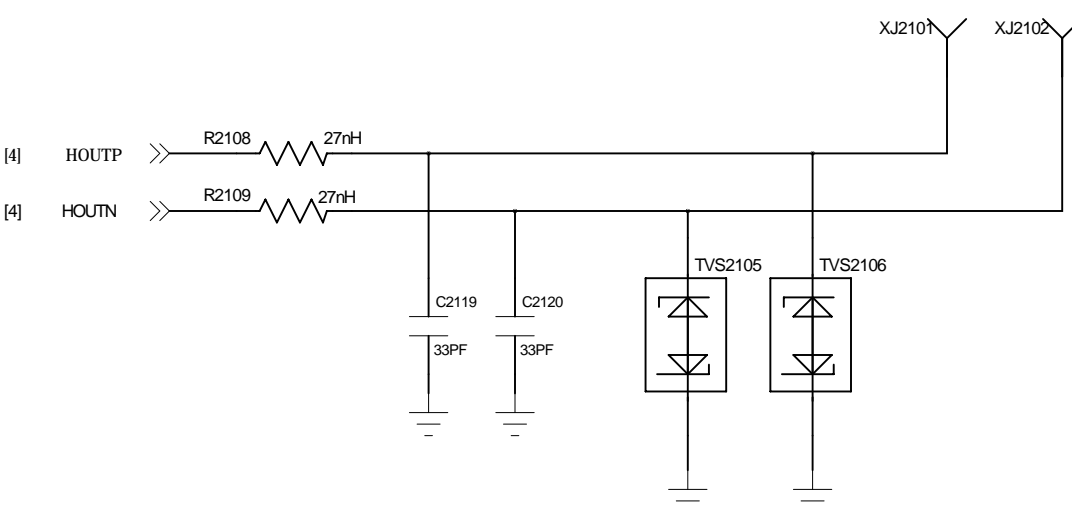
IN=0, COM Connected to NC;
IN=1, COM Connected to NO;

AUXMIC



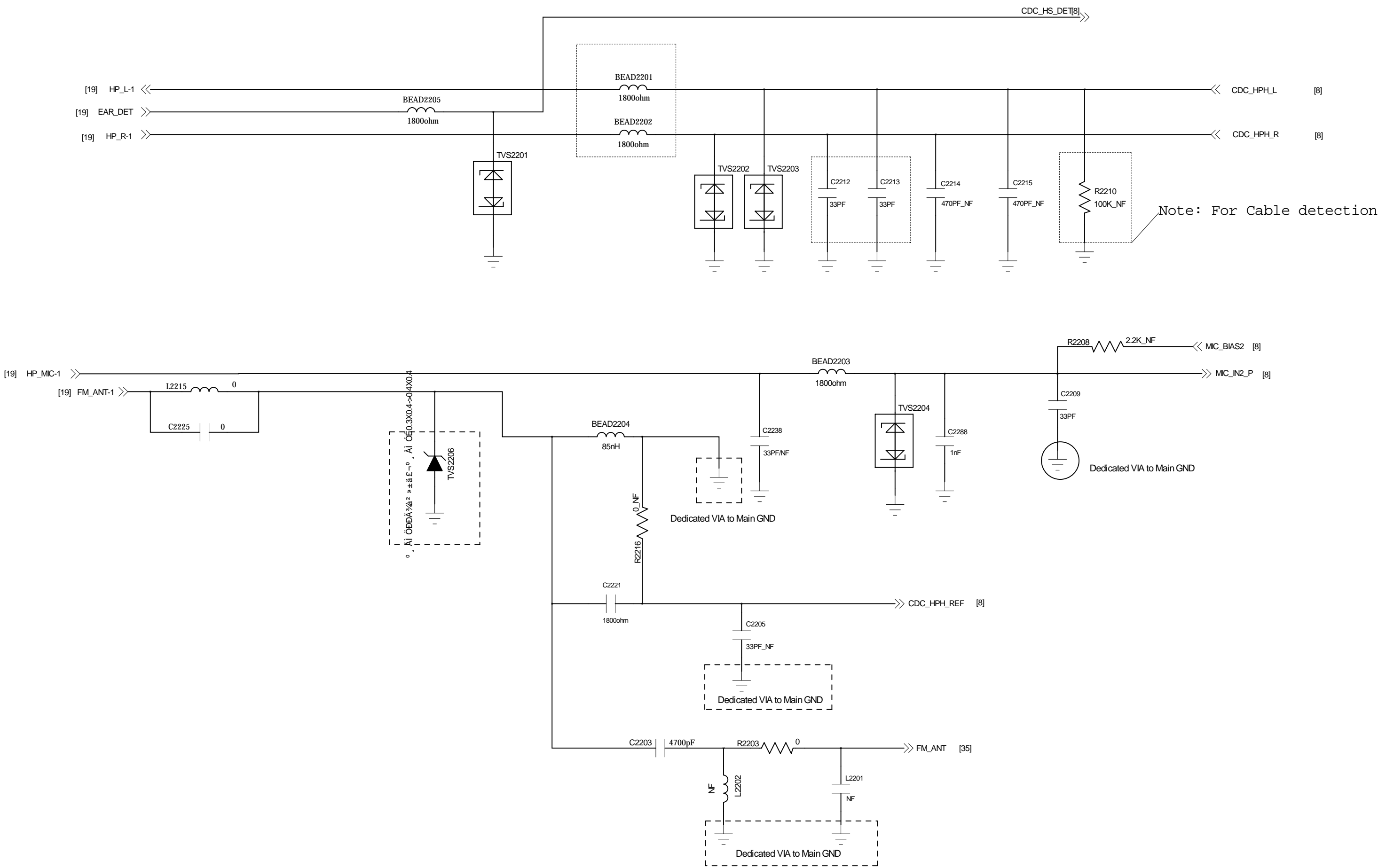
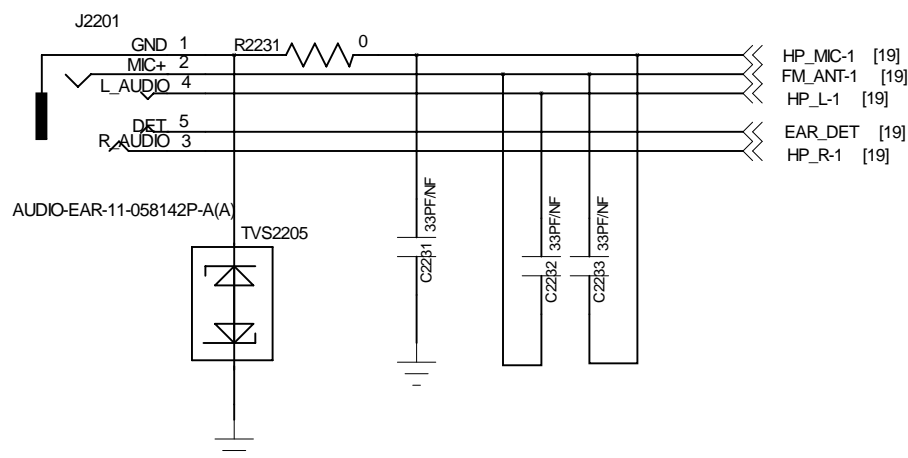
together then single via to main GND

MOTOR



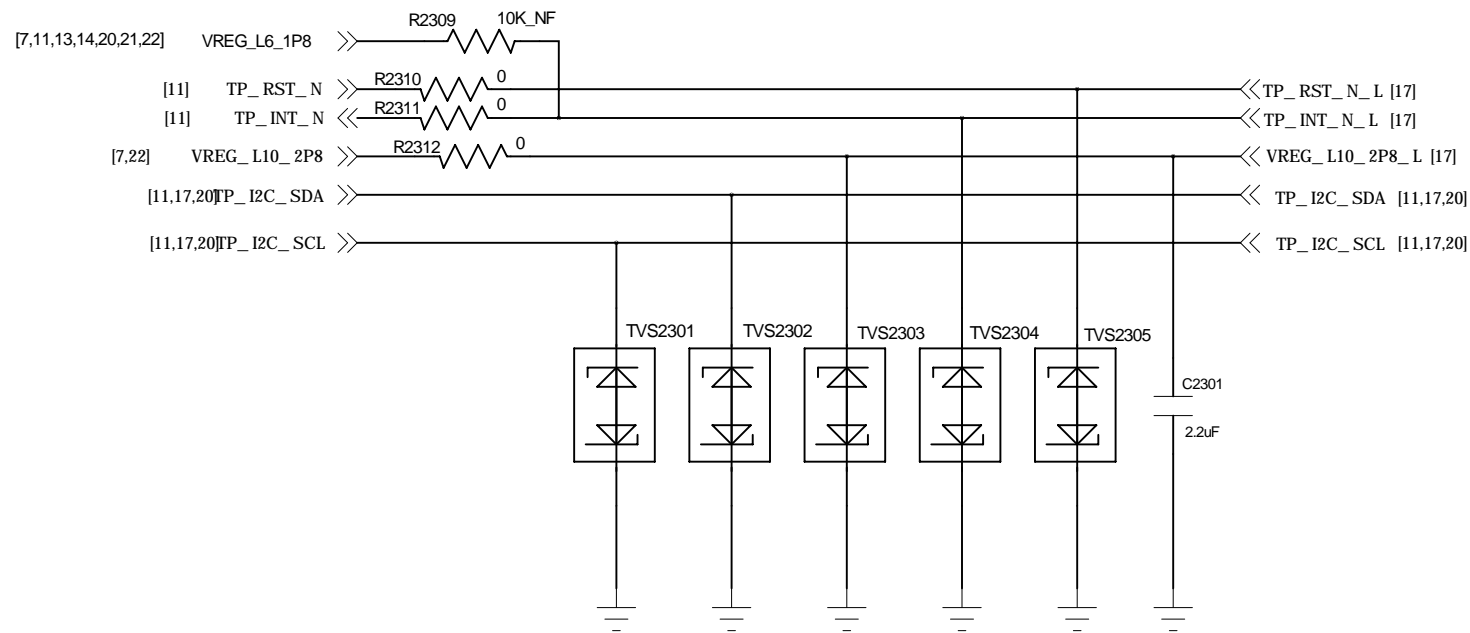
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EARPHONE

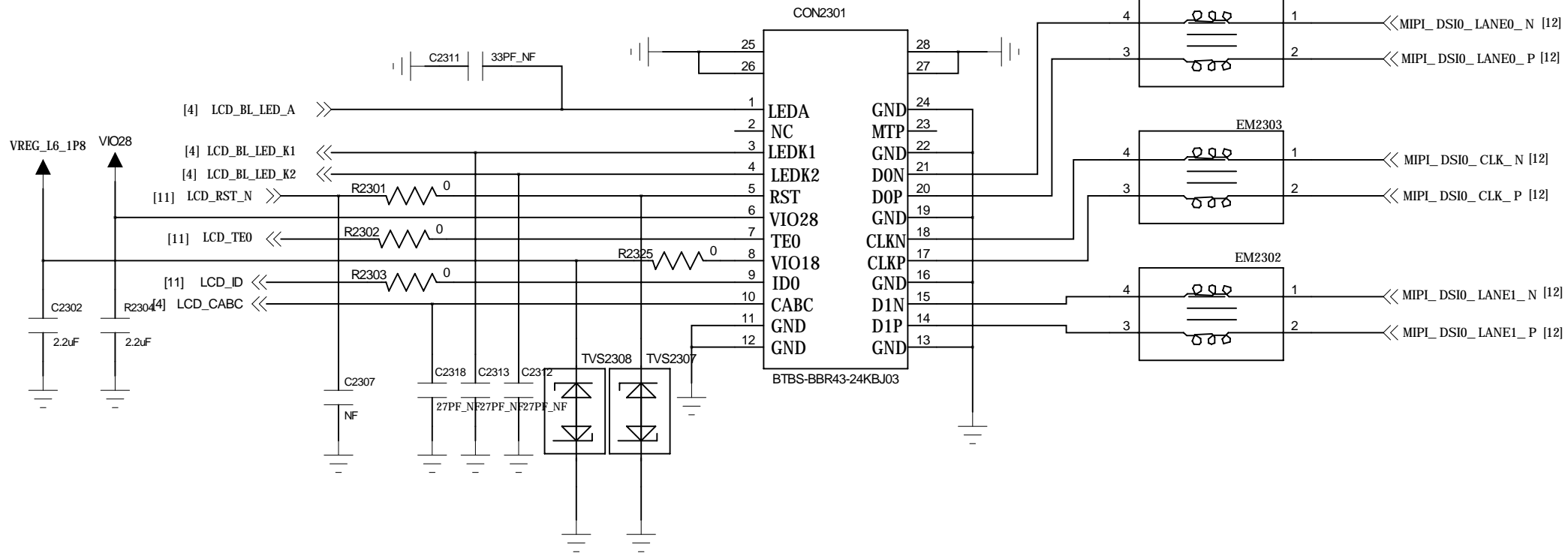


Note: Ferrite beads and their corresponding bypass capacitors on CDC_HPH_L, CDC_HPH_R and CDC_HPH_REF are needed to reduce noise generated by audio/FM concurrency

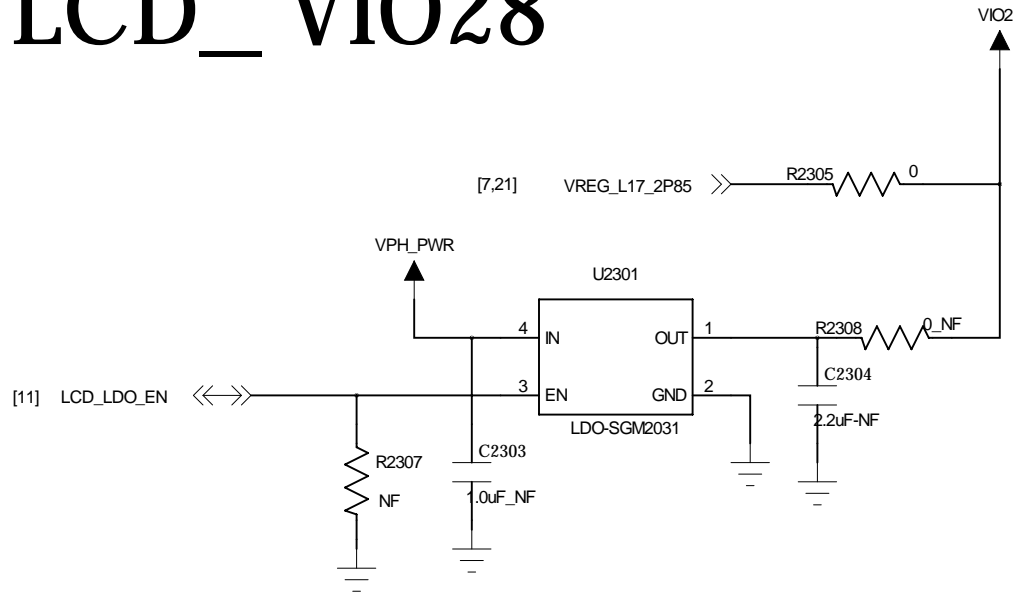
CTP



LCD

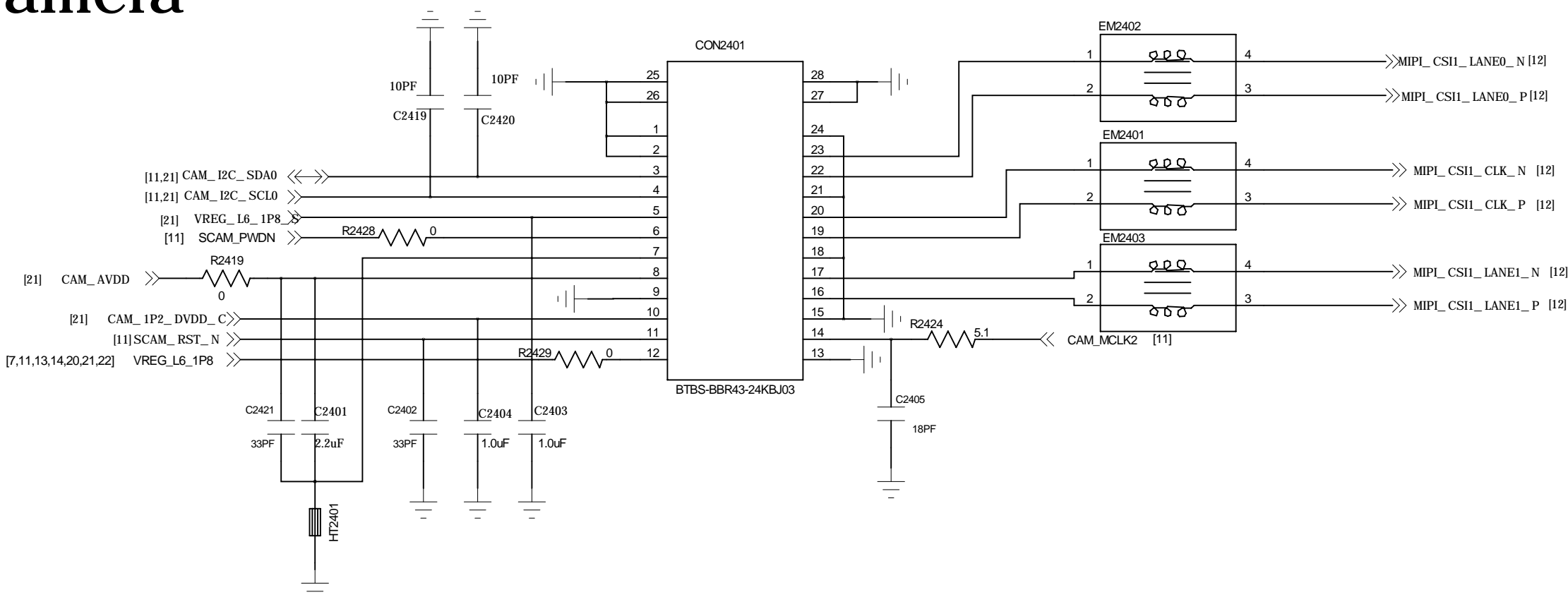


LCD_ VIO28



Note: If best EMI practices are followed for MIPI CSI/DSI signals, there is no need for common mode choke filters. You may choose to have placeholders for common mode depending upon your design constraints.
Extreme care must be taken that no stubs are created by doing so.

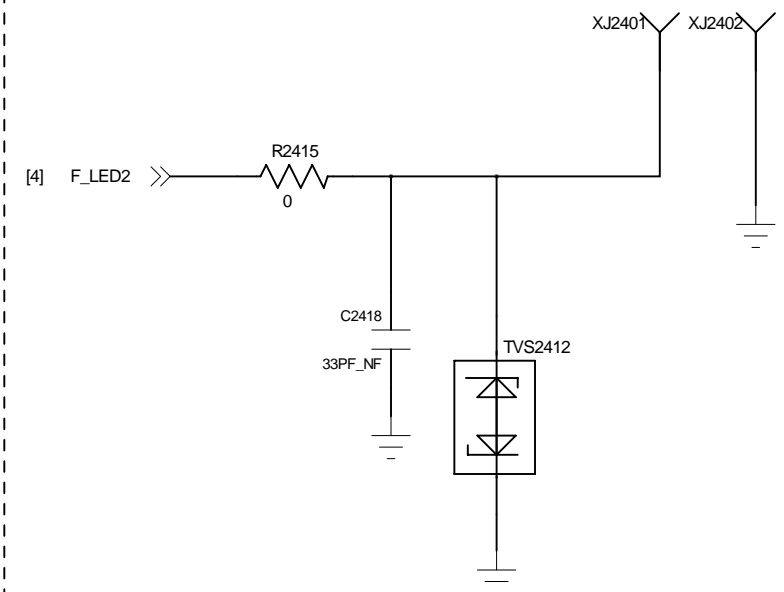
Front Camera



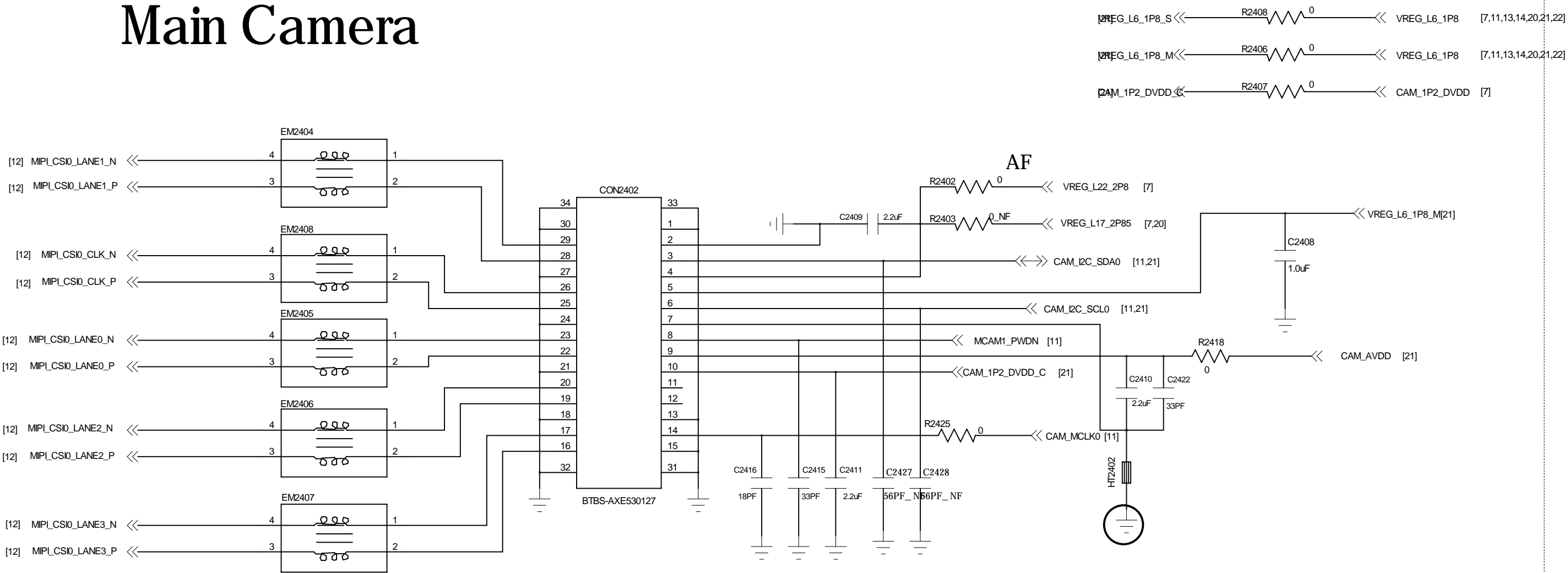
PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
	GND	GND	SDA	SCL	DOVDD	CAM_PWDN (NC)	AGND	AVDD	GND	DVDD	CAM_RST	NC	GND	CMMCLK	GND	ROP1_A	RON1_A	GND	RCP_A	RCN_A	GND	ROP0_A	RON0_A	GND

Main Camera / Sub Camera share power domain design should double check the voltage level is compatible

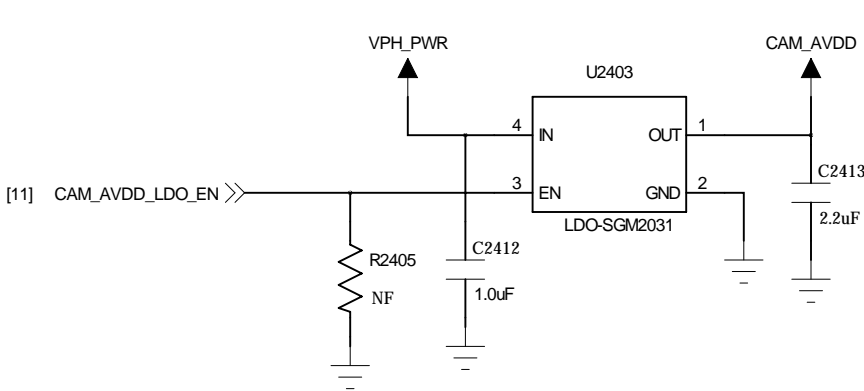
Front Flash LED



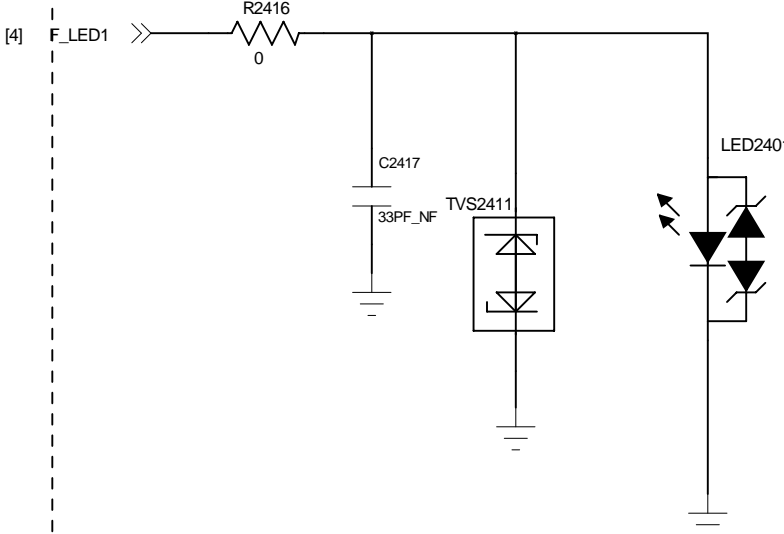
Main Camera



EXT_ AVDD



Main Flash LED



PIN	
1	DGND
2	AF-GND
3	SDA
4	AF-VCC
5	DOVDD
6	SCL
7	AGND
8	PWDN
9	AVDD
10	DVDD
11	NC
12	NC
13	DGND
14	XCLK
15	DGND
16	MDP3
17	MDN3
18	DGND
19	MDP2
20	MDN2
21	DGND
22	MDP0
23	MDN0
24	DGND
25	MCP
26	MCN
27	DGND
28	MDP1
29	MDN1
30	DGND

G-Sensor

The diagram illustrates the electrical connection for a G-Sensor (BMA253) interfaced with a U2501 microcontroller. The U2501 is configured with a 1.8V supply (VREG_L6_1P8) and a 0.1μF bypass capacitor (C2501). The BMA253 is connected to the U2501 via I2C (SDO, SDX, SDY, SDZ, SCL) and interrupt lines (INT1, INT2). The BMA253 is also connected to a 47K_NF resistor and a 47K_NF resistor, which are connected to the VREG_L6_1P8 and GND. The BMA253 is labeled 'SENSOR ACCELER_BMA253'.

U2501 Pin Connections:

- 1: SDO
- 2: SDX
- 12: SDY
- 10: SCL
- 11: INT1
- 5: INT2

BMA253 Pin Connections:

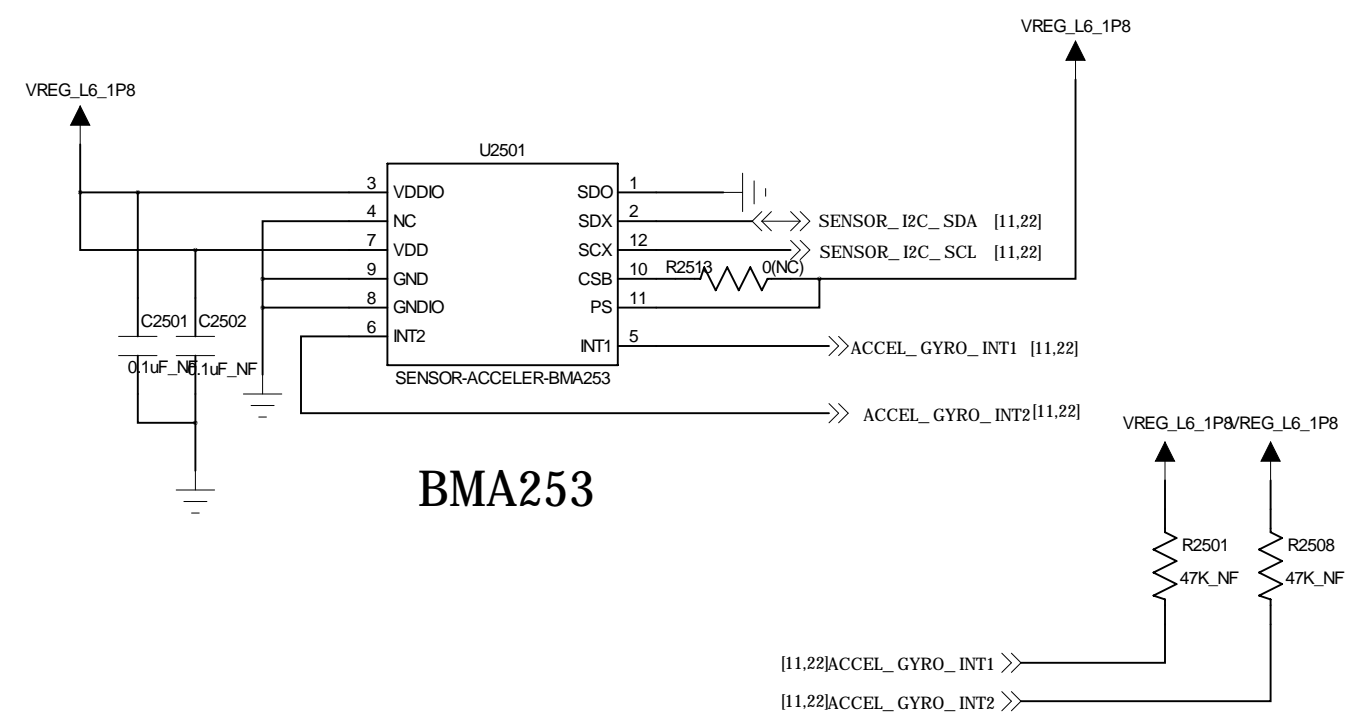
- 3: VDDIO
- 4: NC
- 7: VDD
- 9: GND
- 8: GNDIO
- 6: INT2

Other Components:

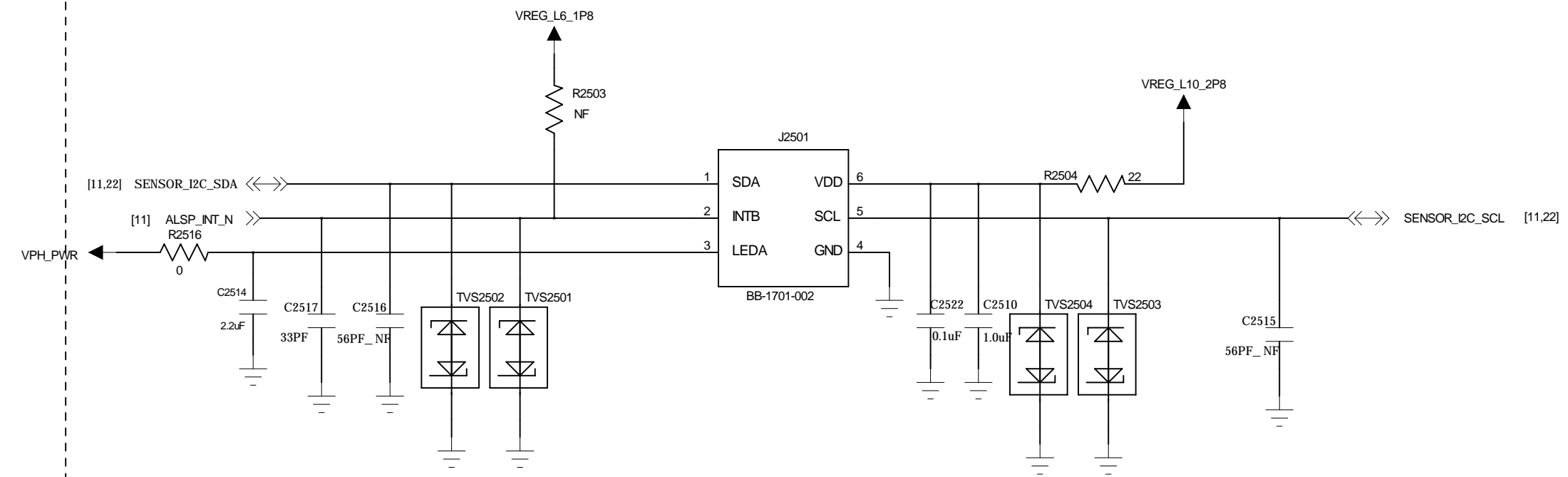
- C2501: 0.1μF
- C2502: 1μF
- R2501: 47K_NF
- R2502: 47K_NF

Signal Labels:

- VREG_L6_1P8
- SENSOR_I2C_SDA [1.22]
- SENSOR_I2C_SCL [1.22]
- ACCEL_GYRO_INT1 [1.22]
- ACCEL_GYRO_INT2 [1.22]
- VREG_L6_1P8/REG_L6_1P8



ALS+PS+IR



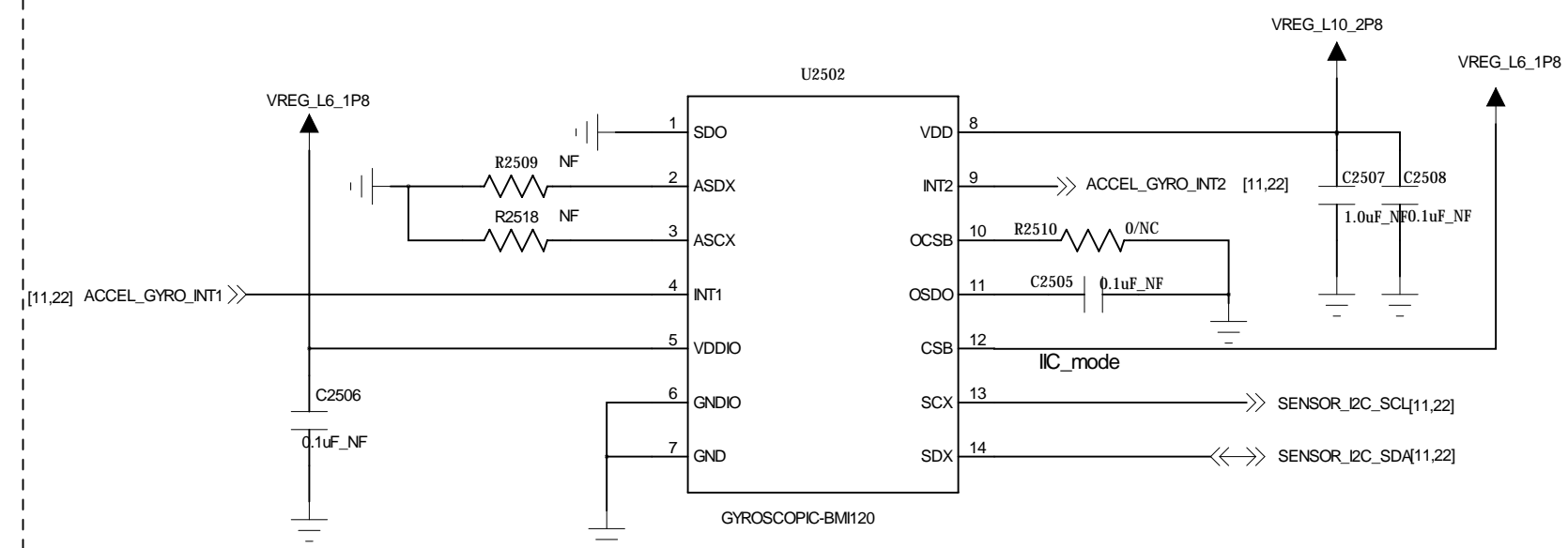
Gyroscope

The diagram illustrates the electrical connections for the Gyroscope (GYROSCOPIC-BM120). The device is shown with its 14 pins and their respective functions:

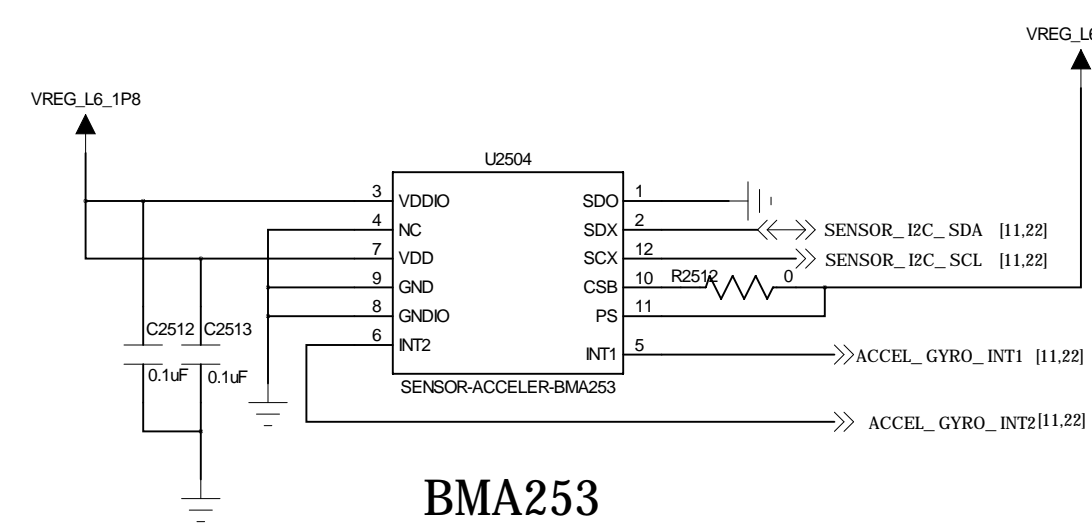
- Pin 1:** SDO (Serial Data Out)
- Pin 2:** ASOX (Analog Signal Output X)
- Pin 3:** ASOY (Analog Signal Output Y)
- Pin 4:** INT1 (Interrupt 1)
- Pin 5:** VDDIO (I/O Supply Voltage)
- Pin 6:** GNDIO (I/O Ground)
- Pin 7:** GND (Ground)
- Pin 8:** VDD (Supply Voltage)
- Pin 9:** INT2 (Interrupt 2)
- Pin 10:** OCSB (Output Control Select B)
- Pin 11:** OSD0 (Output Select 0)
- Pin 12:** CSB (Chip Select B)
- Pin 13:** SCX (Serial Clock X)
- Pin 14:** SDX (Serial Data X)

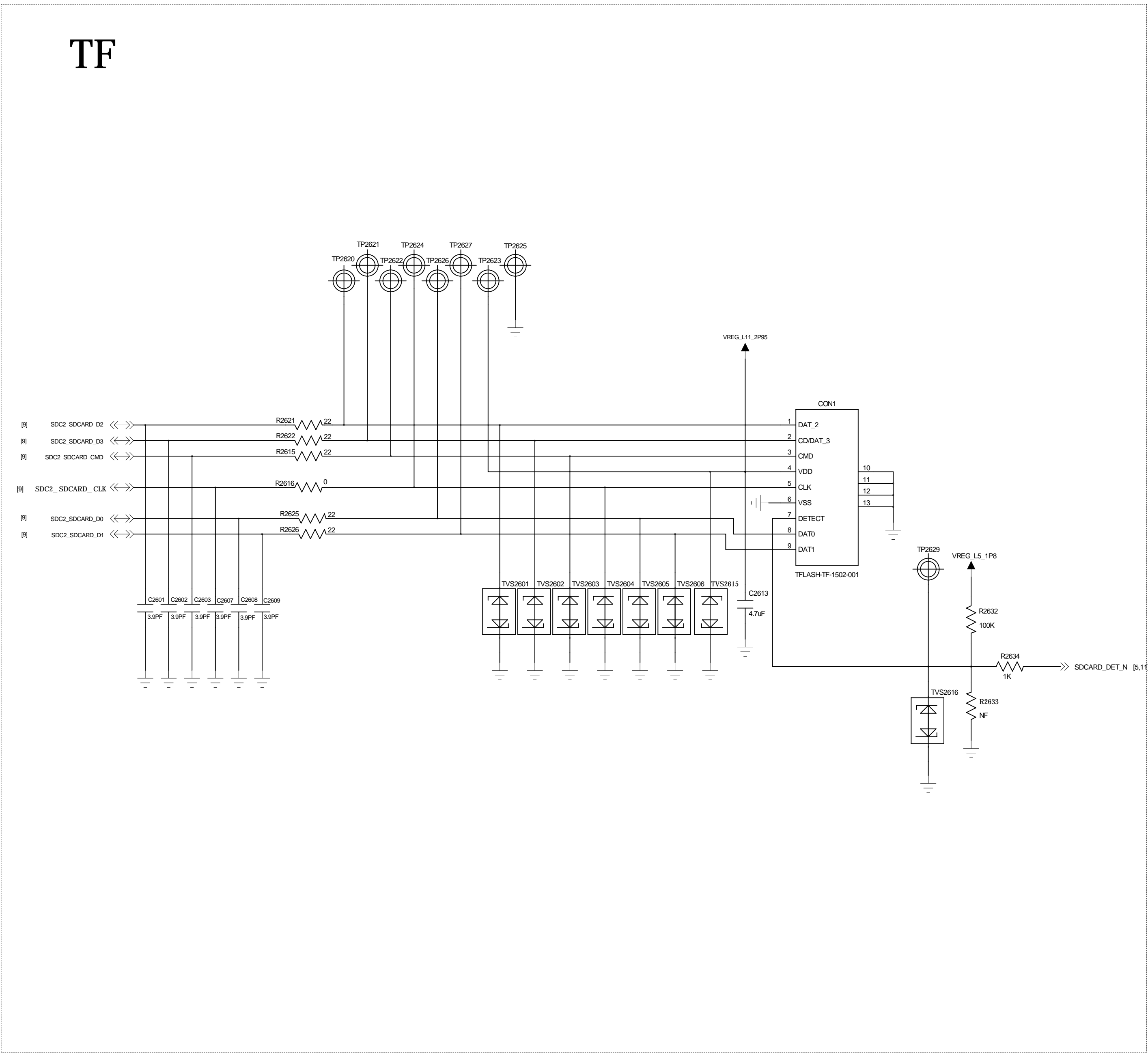
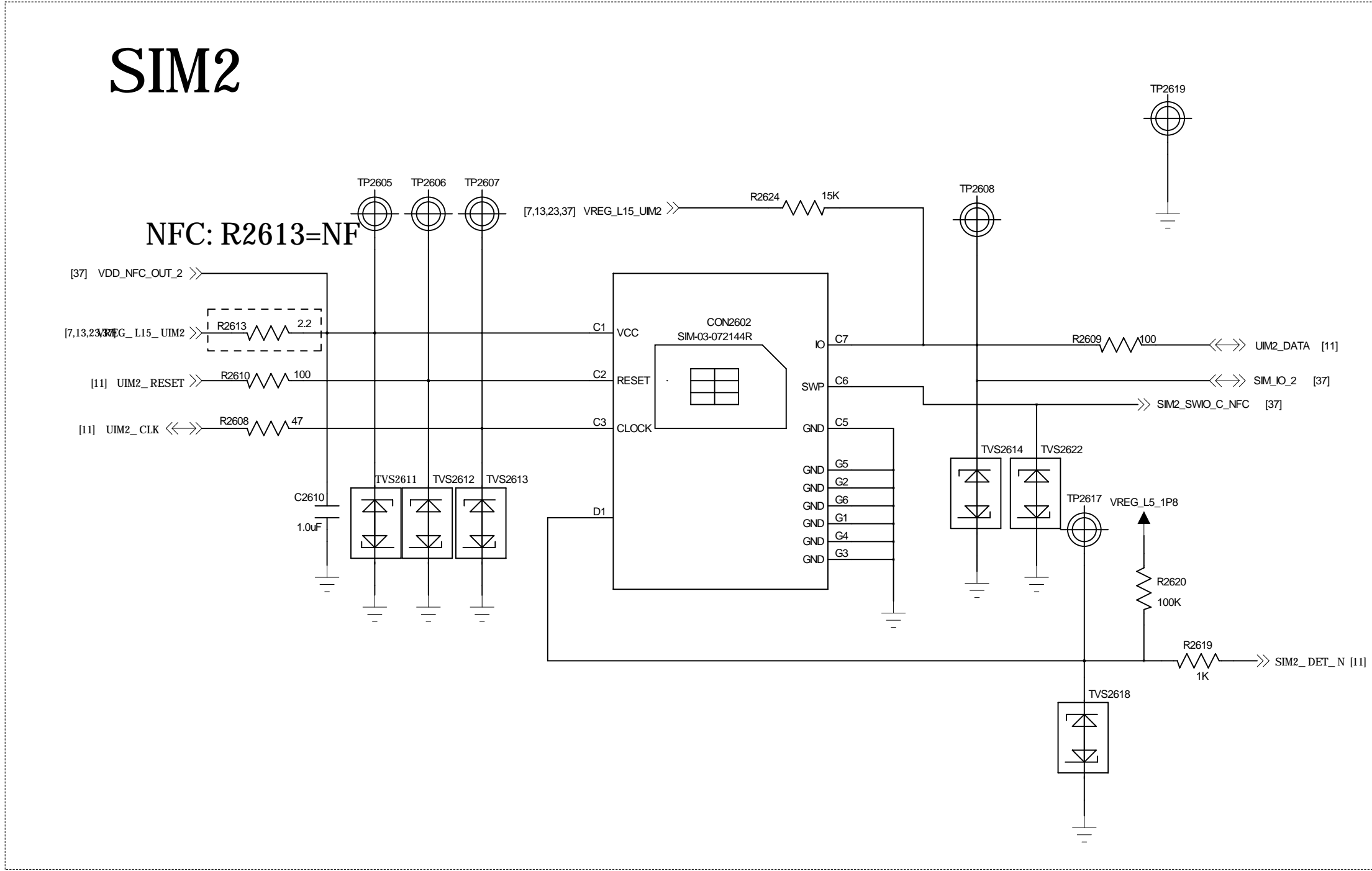
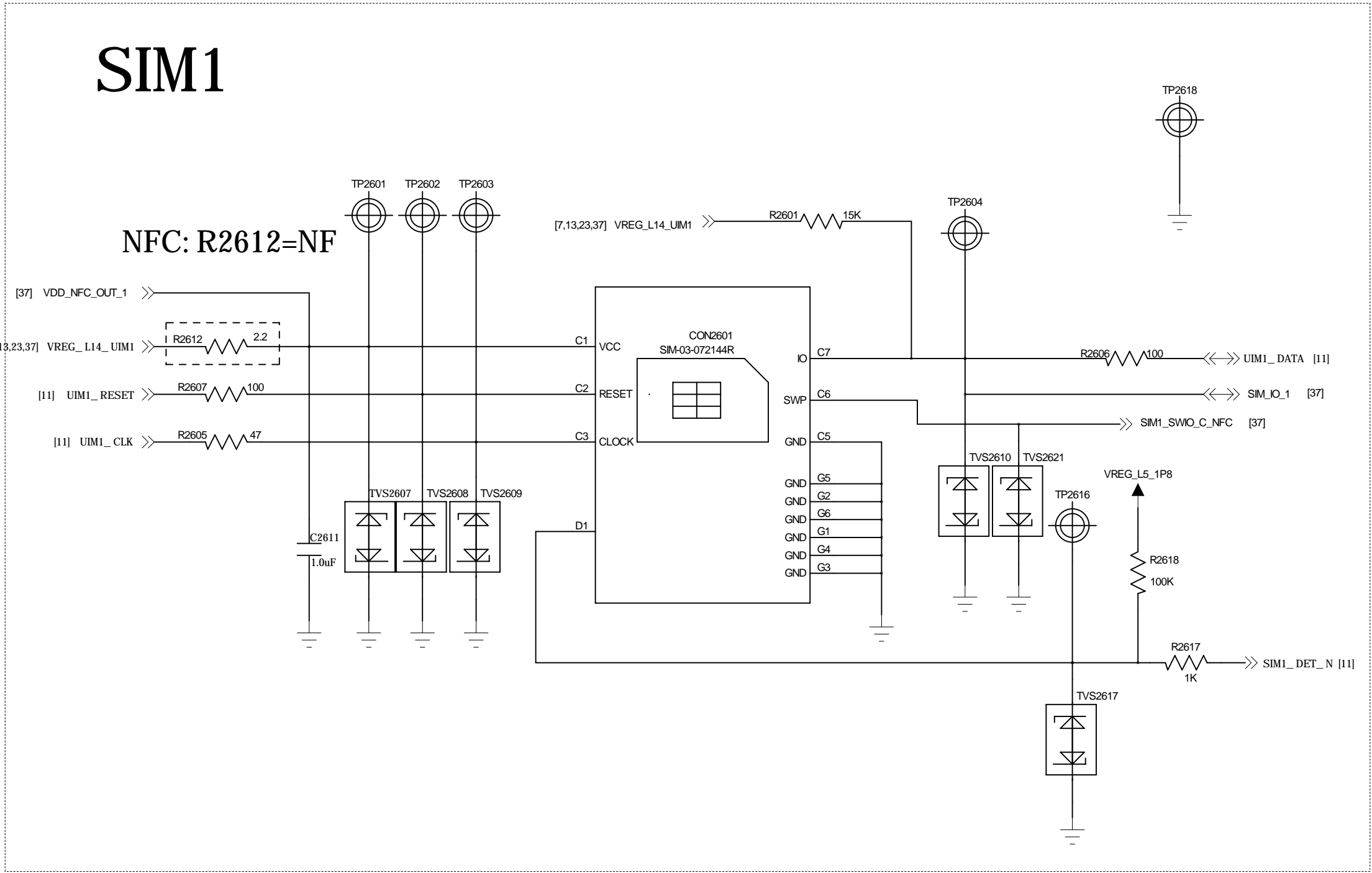
The diagram shows the following connections:

- Power Supply:** VREG_L6_1P8 is connected to VDD (Pin 8). VREG_L10_2P8 is connected to VDD (Pin 8). VREG_L6_1P8 is also connected to VDDIO (Pin 5).
- Grounding:** GND (Pin 7) is connected to the common ground. GNDIO (Pin 6) is connected to the common ground.
- Signal Connections:**
 - INT1 (Pin 4) is connected to the ACCEL_GYRO_INT1 signal.
 - INT2 (Pin 9) is connected to the ACCEL_GYRO_INT2 signal.
 - SCX (Pin 13) is connected to the SCX signal.
 - SDX (Pin 14) is connected to the SDX signal.
- Internal Components:**
 - The device contains an I2C mode block.
 - Resistors R2509, R2510, and R2518 are shown.
 - Capacitors C2506, C2507, C2508, and C2509 are shown.
 - The device is labeled GYROSCOPIC-BM120.



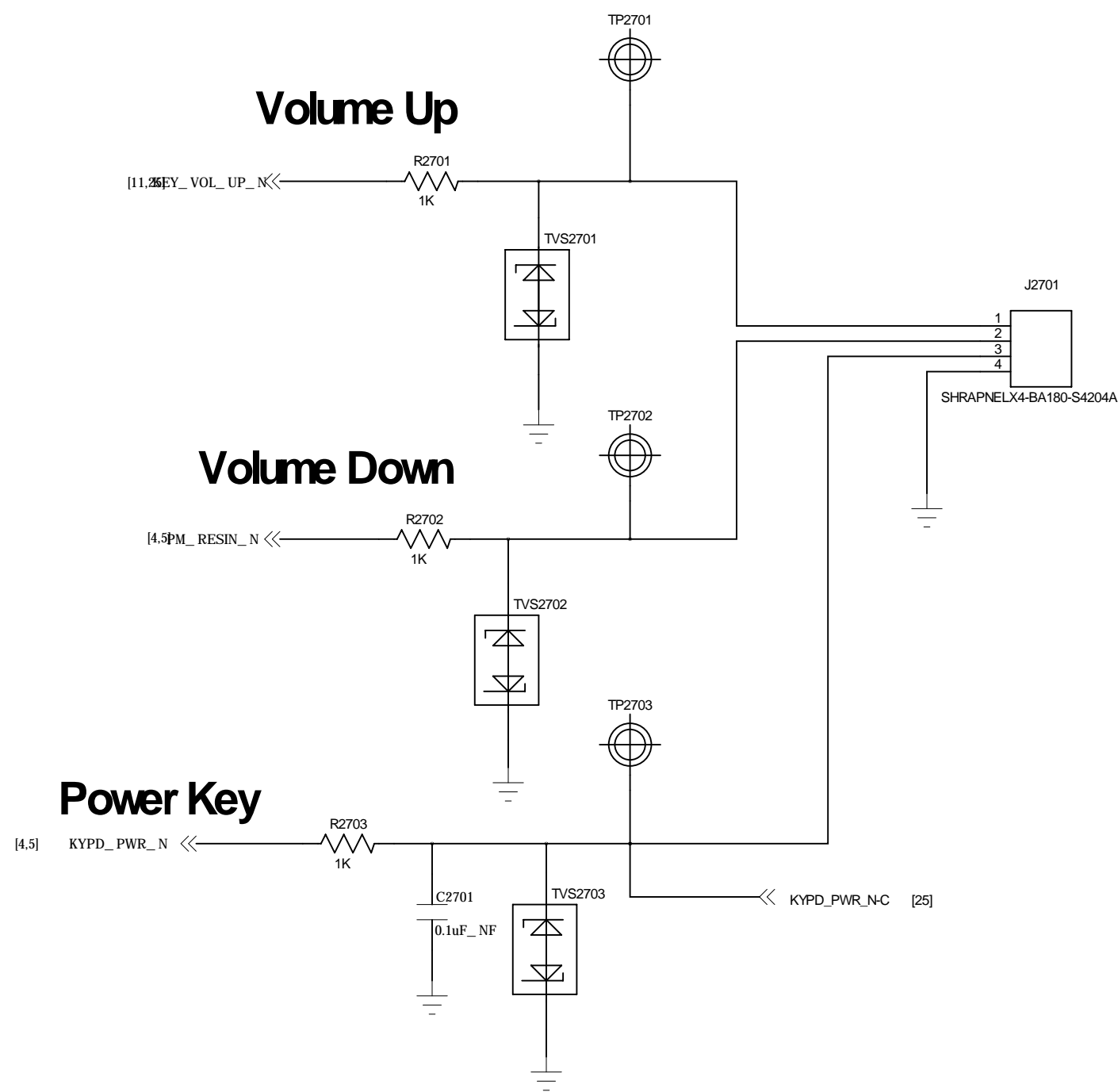
G-Sensor



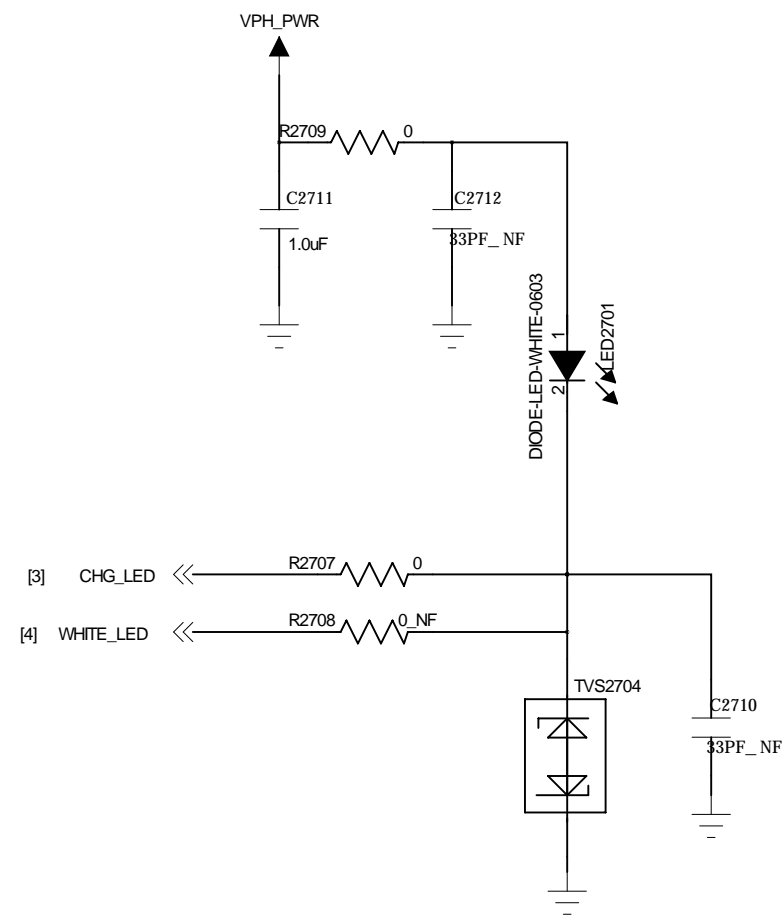


KEYPAD

Signal	Description
KEY_VOL_UP_N	Volume Up
PM_RESIN_N	Volume Down
KYPD_PWR_N	POWER_ON
PM_RESIN_N + KYPD_PWR_N	Hardware Reset



INDICATOR LED



Title

Sheet

Size

Name

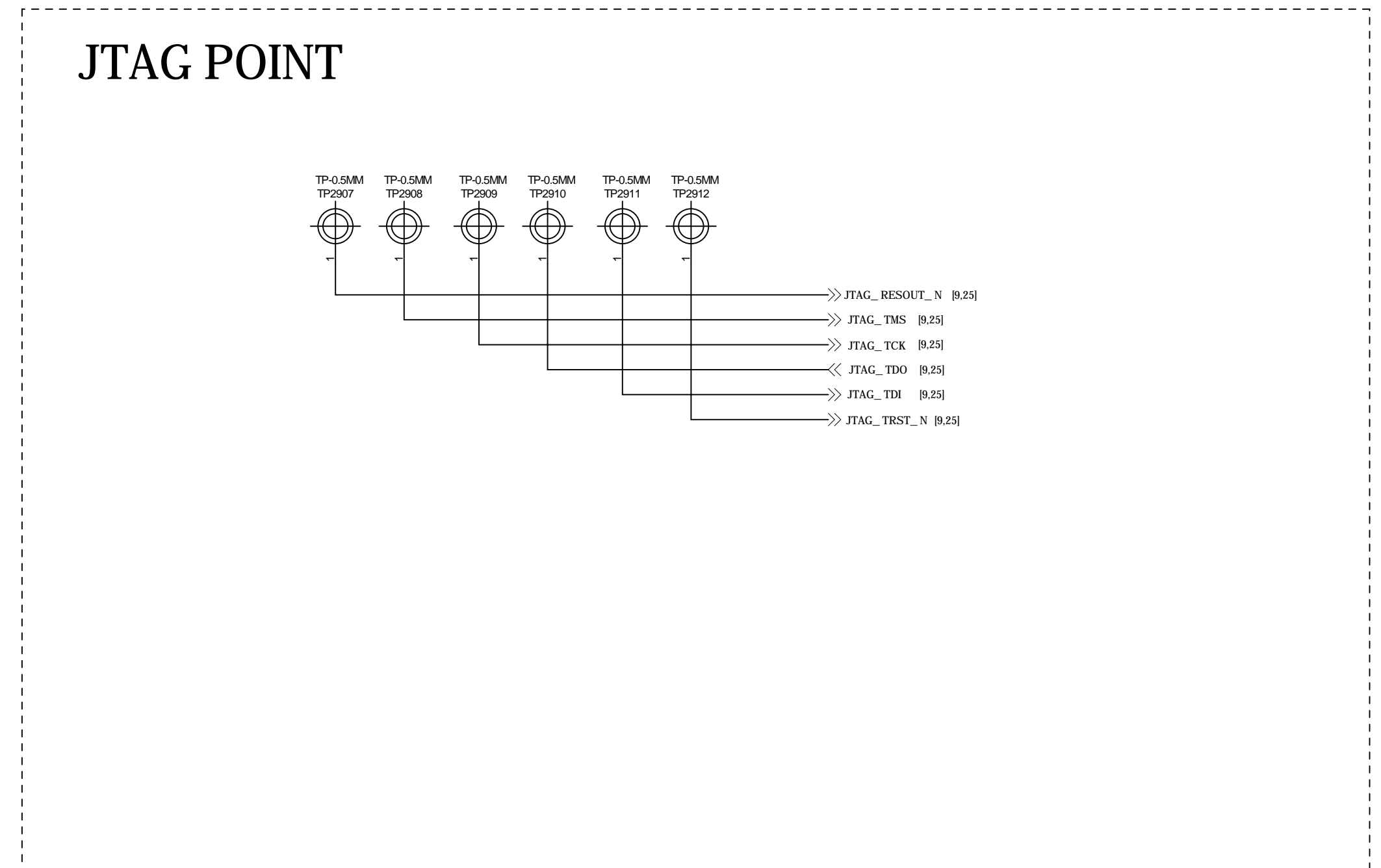
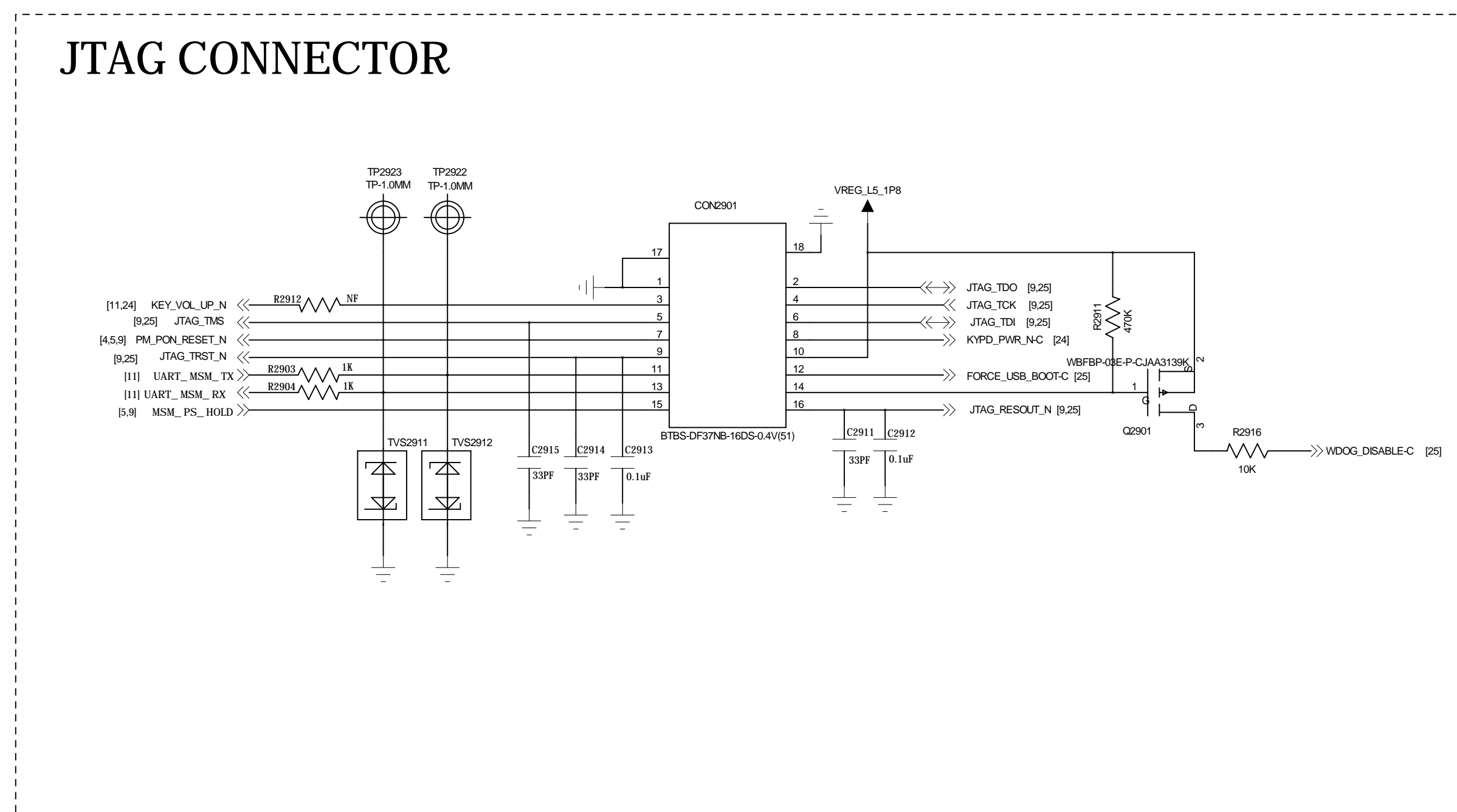
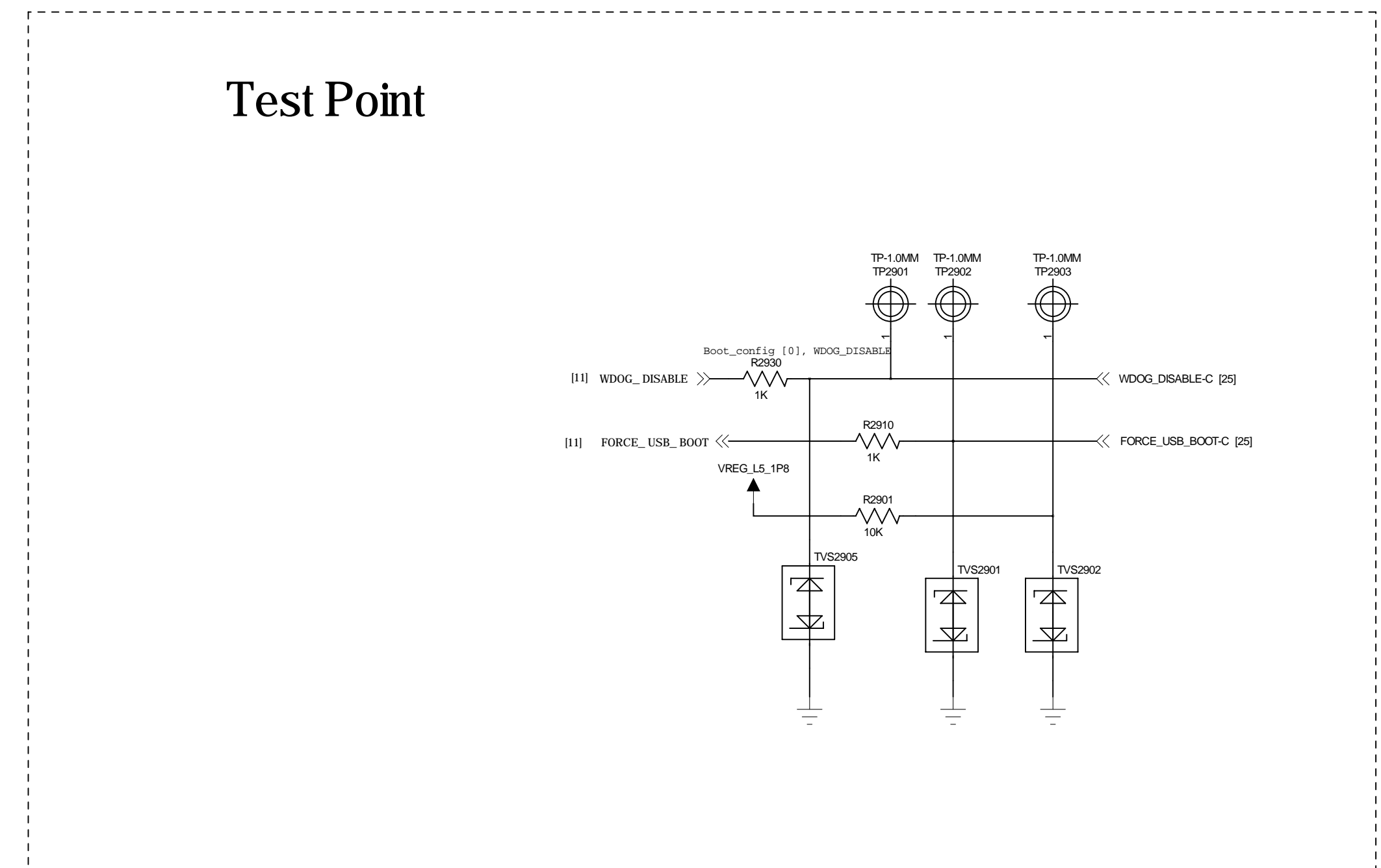
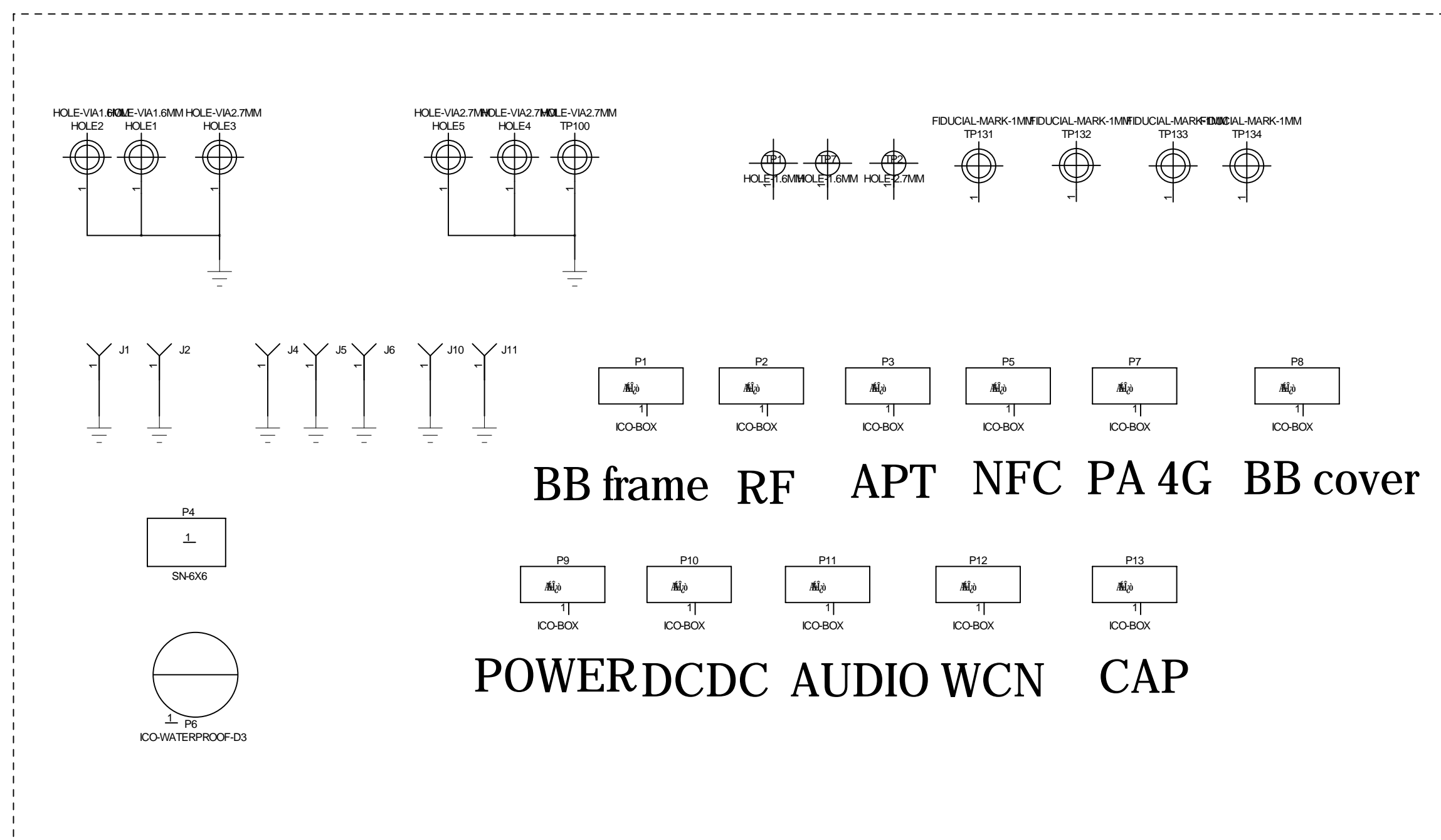
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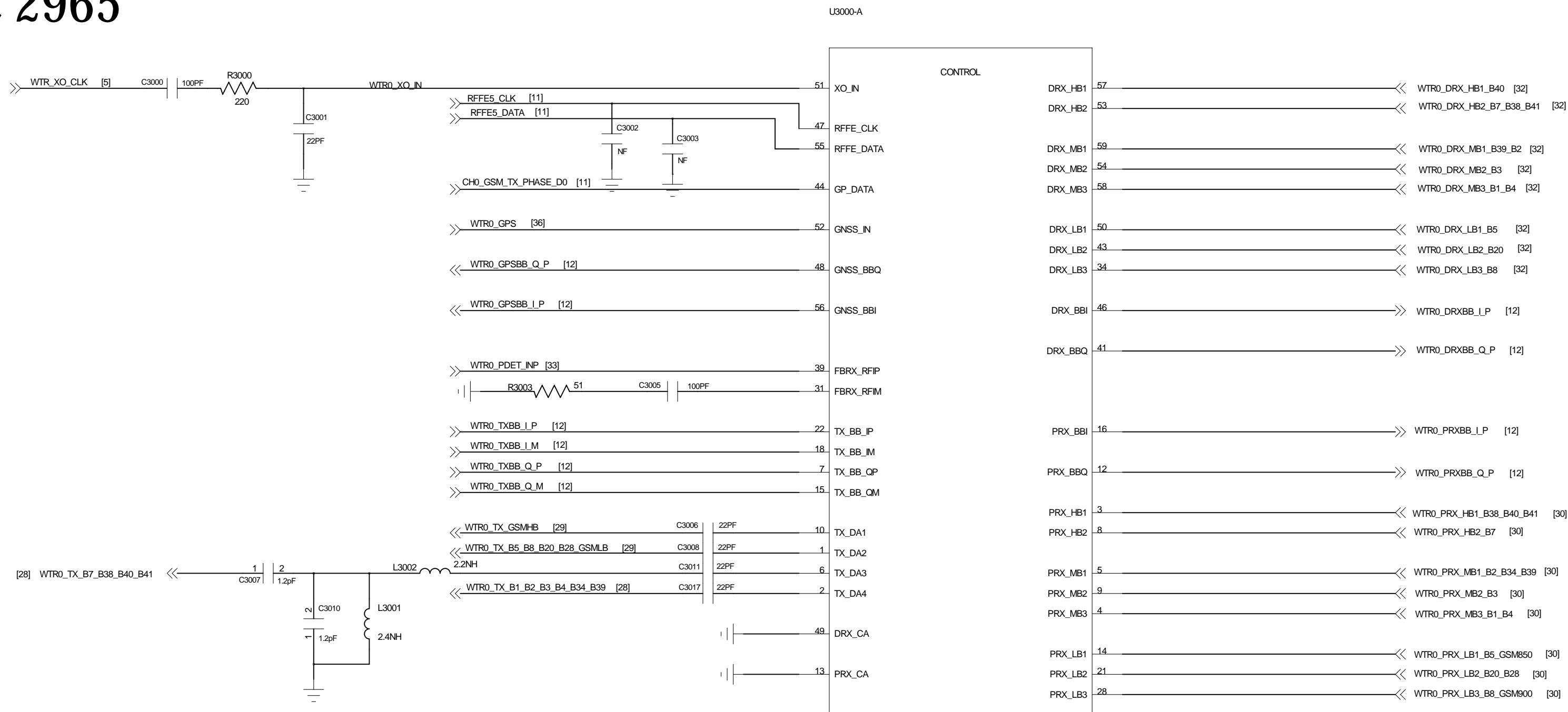
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of

Rev



WTR 2965



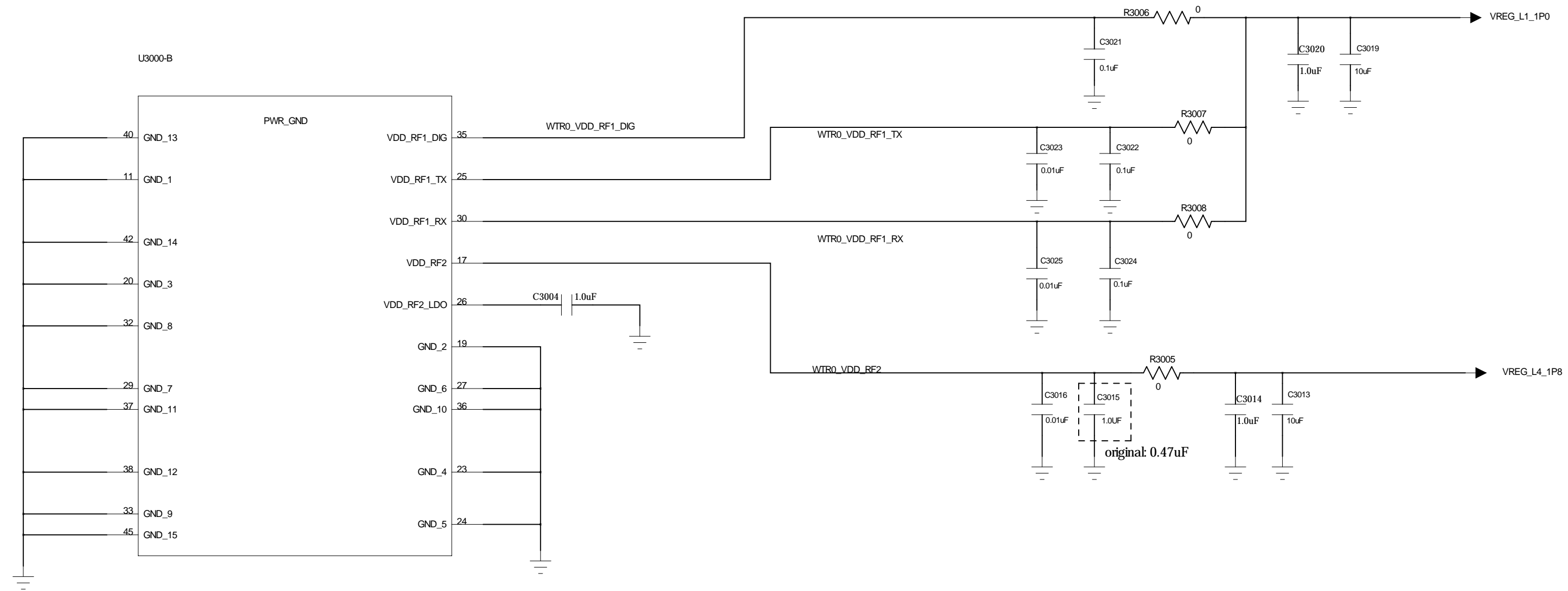
WTR2965 Tx port mapping							
RF port	GSM	CDMA	WCDMA	LTE-FDD	LTE-TDD		TD-SCDMA
Tx_DA1	850, 900, 1800, 1900	0, 10	8, 11	8, 11, 12, 13, 17, 21, 28			34, 39
Tx_DA2	850, 900		5, 6, 8, 19	5, 6, 8, 18, 19, 20, 26, 27, 28			39, 41
Tx_DA3				7, 30			38, 40, 41
Tx_DA4	1800, 1900	1, 6, 14, 15	1, 2, 3, 4, 9, 10, 11, 25	1, 2, 3, 4, 9, 10, 11, 21, 25, 28			34, 39

Note:RX ports have DC at the pin,
so it need DC block,please make sure
there is no DC short to other voltages and GND

Rx port mapping

WTR2965							
	CDMA	GSM	WCDMA	LTE-FDD	TD-SCDMA	LTE-TDD	Remarks
Prx_LB1	BC0,10	850,900 850 SA/Wless, 900 SA/Wless	5, 6, 8, 19	5, 6, 8, 18, 19, 26, 27			SAWless and SAW mode is not supported at the same time
Prx_LB2				12, 13, 17, 20, 28			
Prx_LB3	BC0,10	850, 900 1900	5, 8	5, 6, 8, 13, 18, 19, 20, 26, 27, 28, 29			
Prx_MB1	BC15 BC1,14	1800 SA/Wless, 1900 SA/Wless	2, 4, 10, 11, 25	2, 4, 10, 11, 21, 25, 32	34 SA/SA/Wless 39 SA/SA/Wless	34 SA/SA/Wless 39 SA/SA/Wless	SAWless and SAW mode is not supported at the same time
Prx_MB2	BC1,14 BC6, 15	1800, 1900	2, 3, 9, 25	2, 3, 9, 25	34, 39	34, 39	
Prx_MB3		1800	1, 3, 4, 9, 10	1, 3, 4, 9, 10, 66			
Prx_HB1				30		38, 40, 41	
Prx_HB2				7		38, 41	

	CDMA	GSM	WCDMA	LTE-FDD	TD-SCDMA	LTE-TDD	Remarks
Drx_LB1	BC0, 10	850, 900	5, 6, 8, 19	5, 6, 8, 18, 19, 26, 27			
Drx_LB2				12, 13, 17, 20, 28			
Drx_LB3	BC0, 10	850, 900	5, 8	5, 6, 8, 13, 18, 19, 20, 26, 27, 28, 29			
Drx_MB1	BC15, BC1,14	1900	2, 4, 10, 11, 25	2, 4, 10, 11, 21, 25, 32	34, 39	34, 39	
Drx_MB2	BC1, 14	1800, 1900	2, 3, 9, 25	2, 3, 9, 25	34, 39	34, 39	
Drx_MB3	BC6, 15	1800	1, 3, 4, 9, 10	1, 3, 4, 9, 10, 66			
Drx_HB1				30		38, 40, 41	
Drx_HB2				7		38, 41	



PRIMARY_ANT

Title		
Sheet		
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3/4G PA

Band7

Band40

Band4

Band3

Band1

Band2

Band5/BC0

Band20/28A

Band8

Band28B

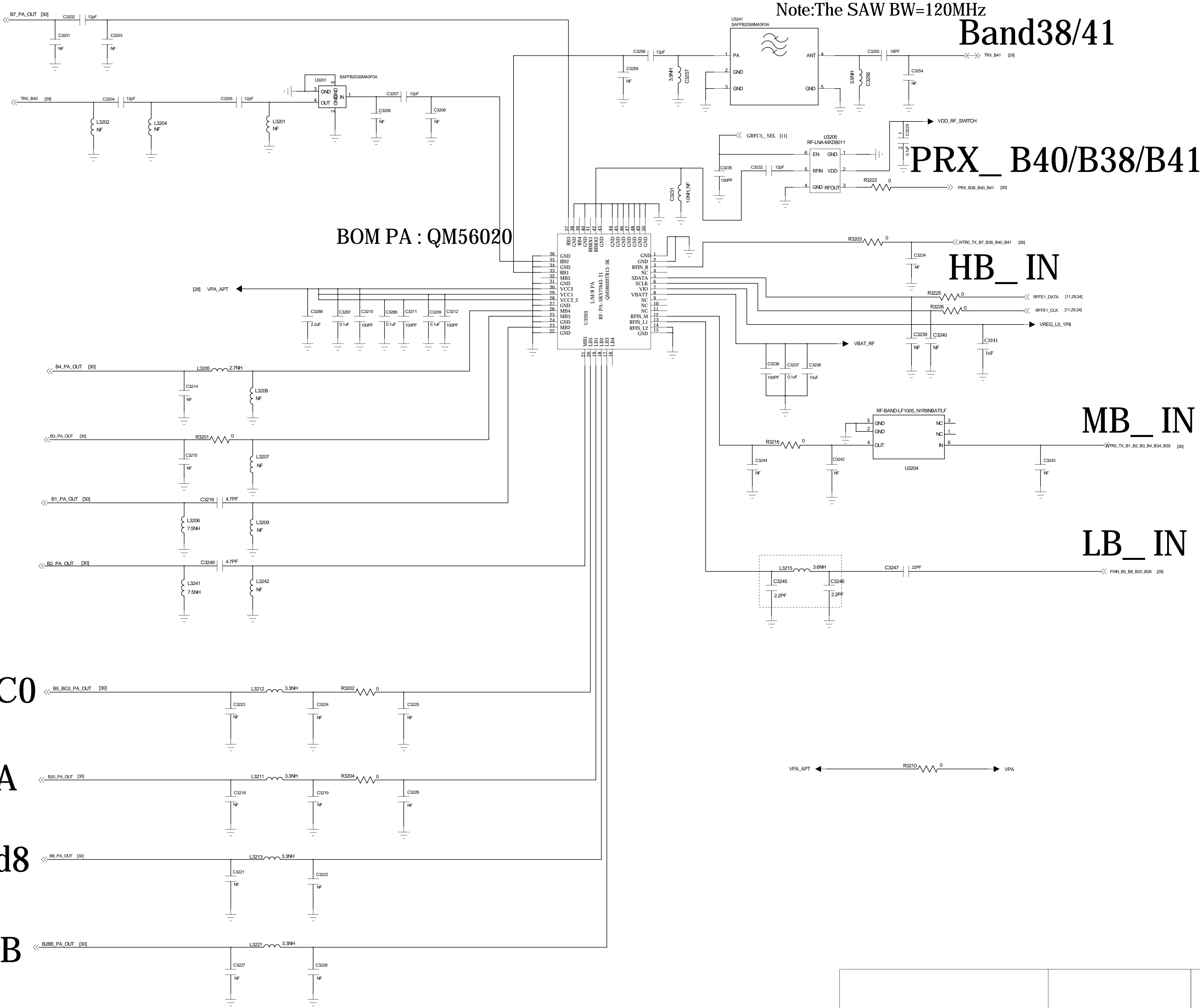
Band38/41

PRX_ B40/B38/B41

HB_IN

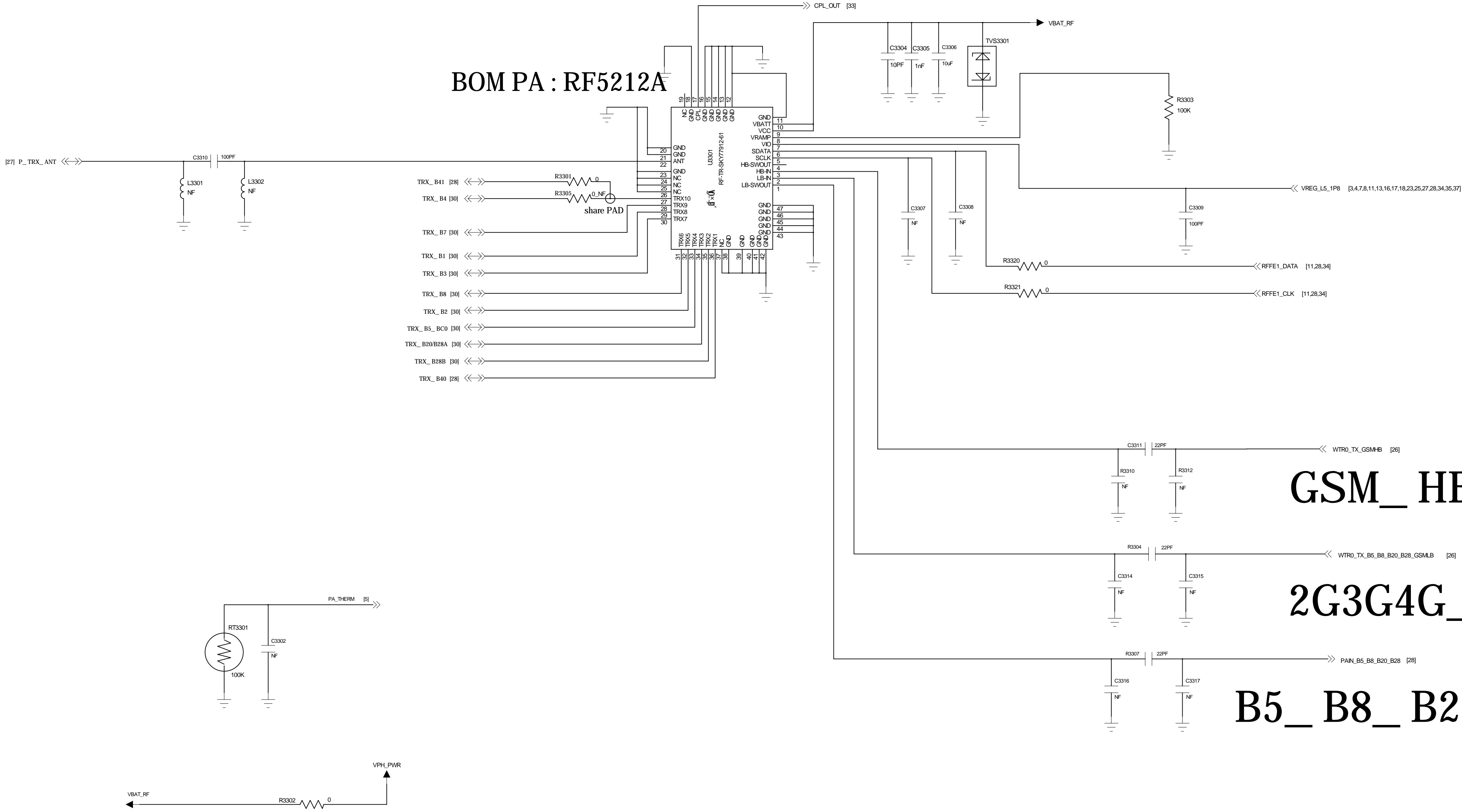
MB_IN

LB_IN



2G PA

BOM PA : RF5212A

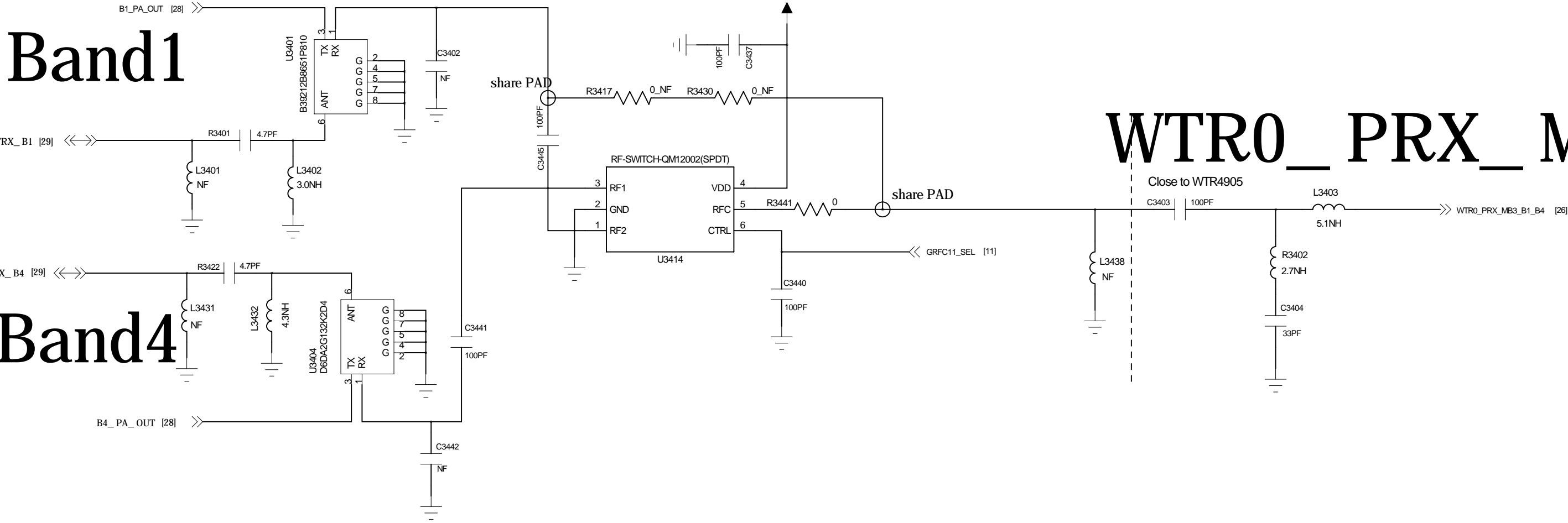


GSM HB

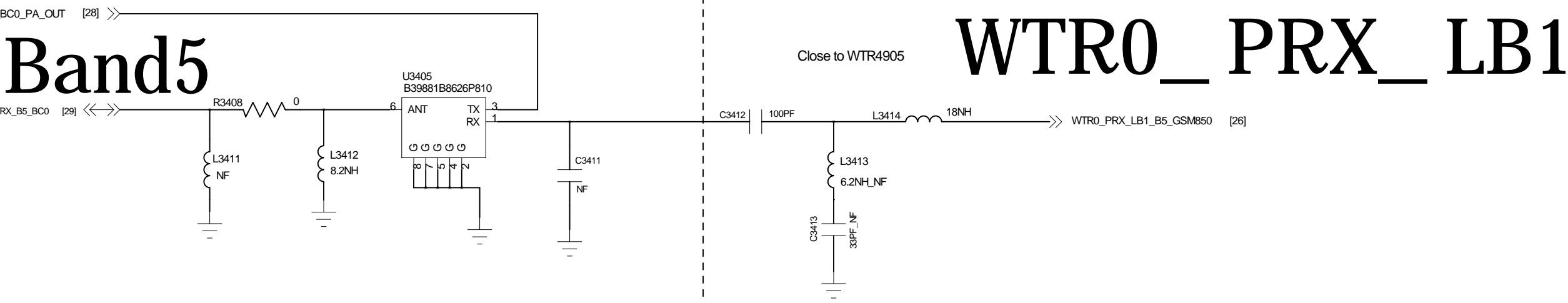
2G3G4G LB

B5 B8 B20 B28

Band1

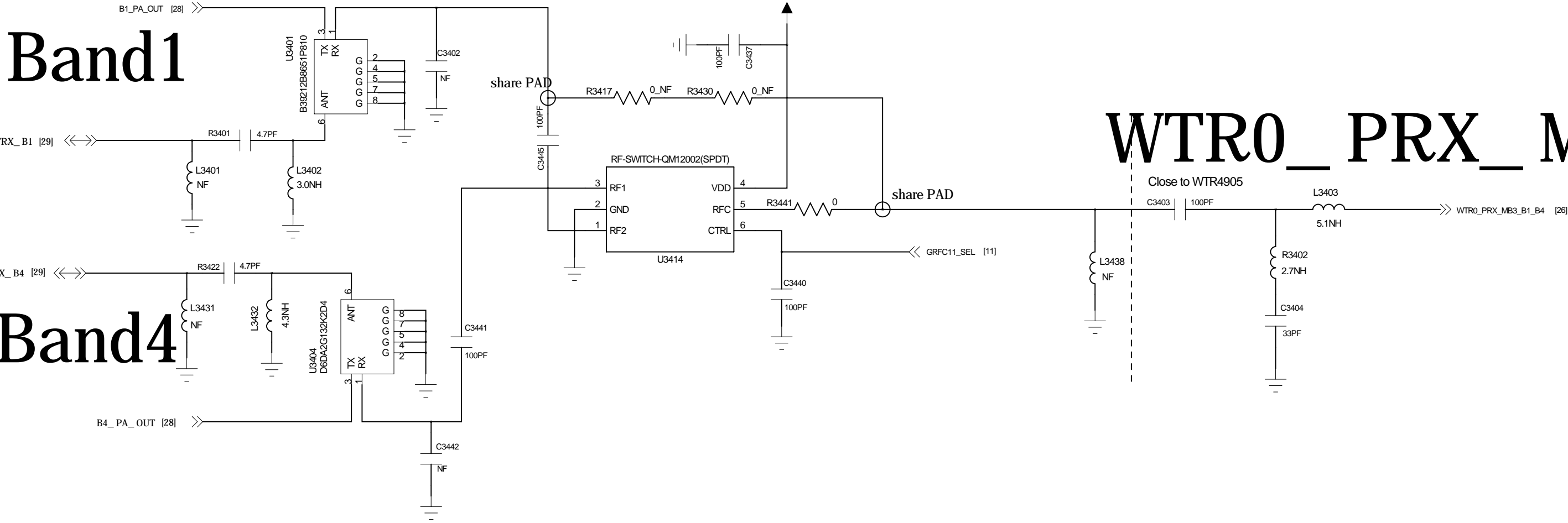


Band5



WTR0_PRX_LB1

Band4

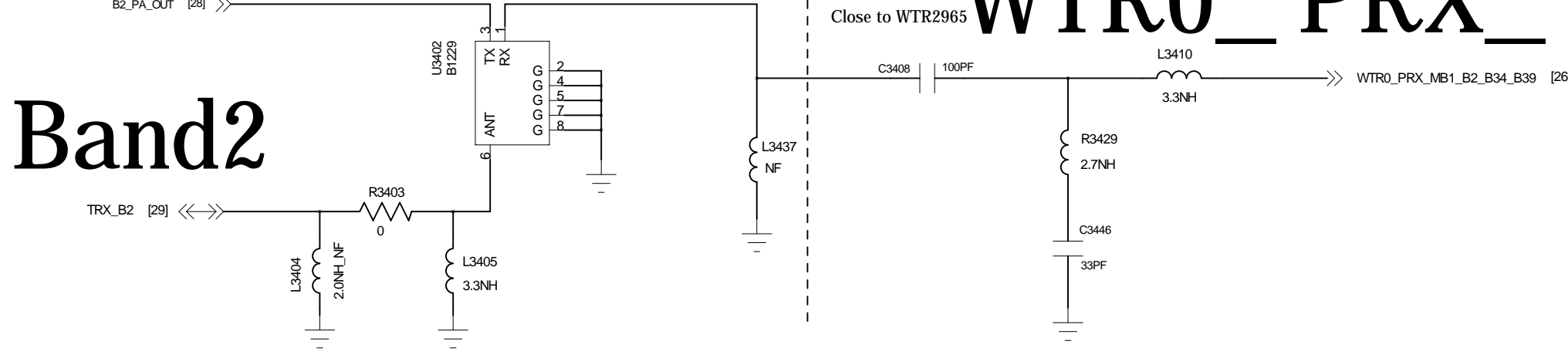


WTR0_PRX_HB2



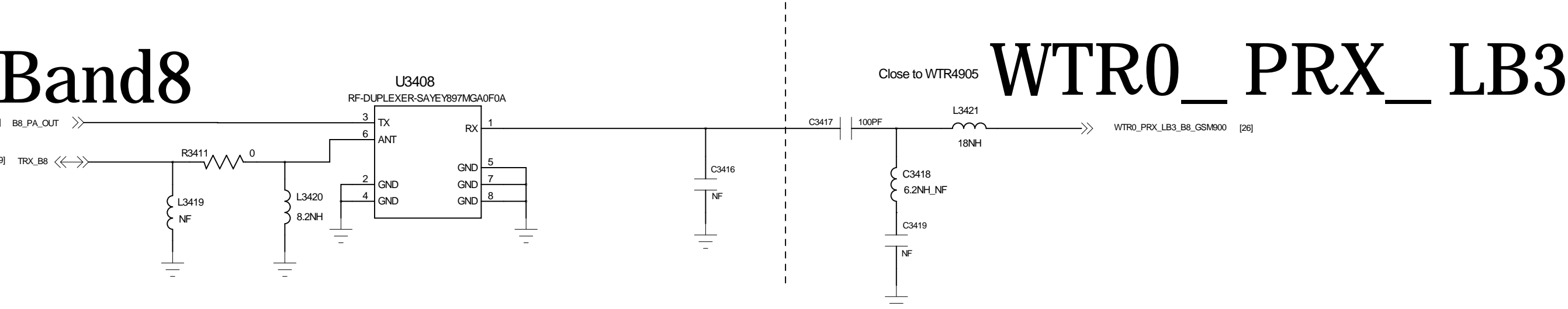
Band7

Band2



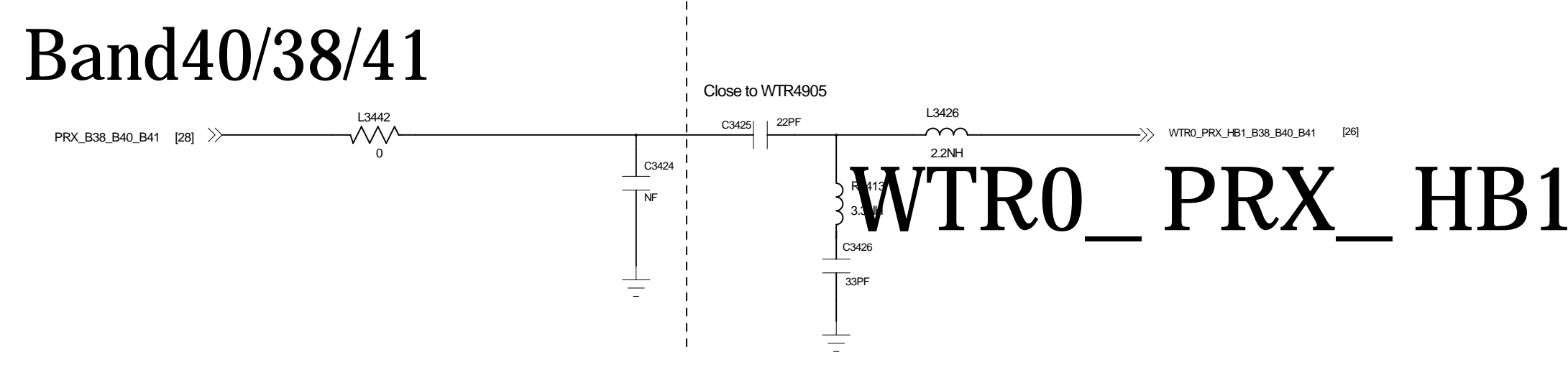
WTR0_PRX_MB1

Band8



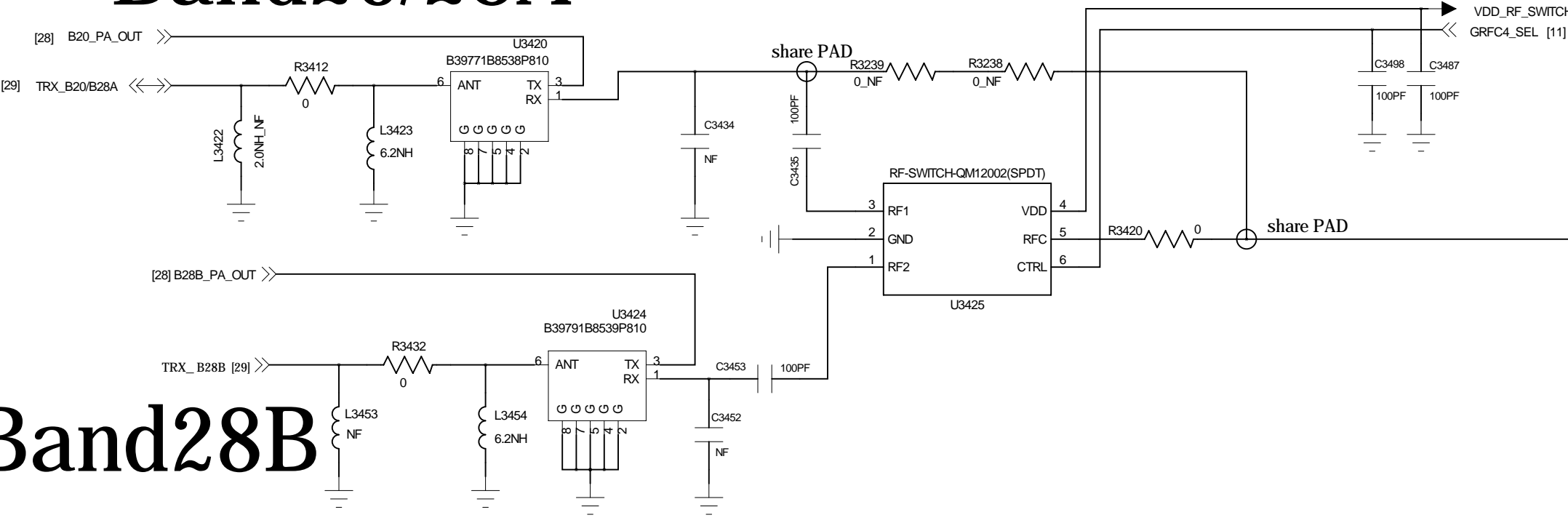
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Band40/38/41



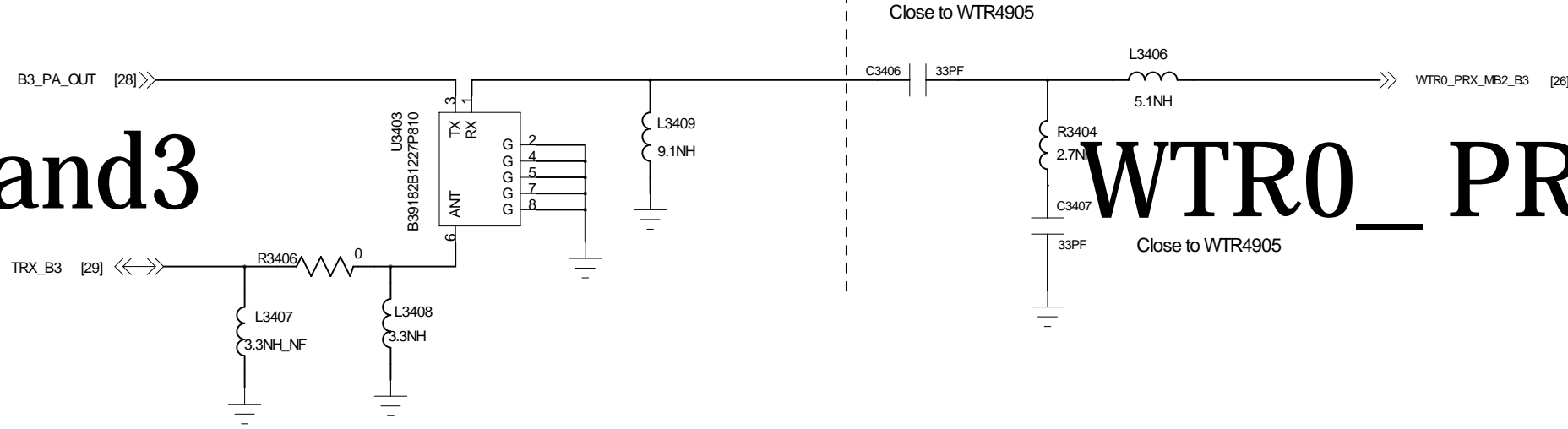
WTR0_PRX_HB1

Band20/28A



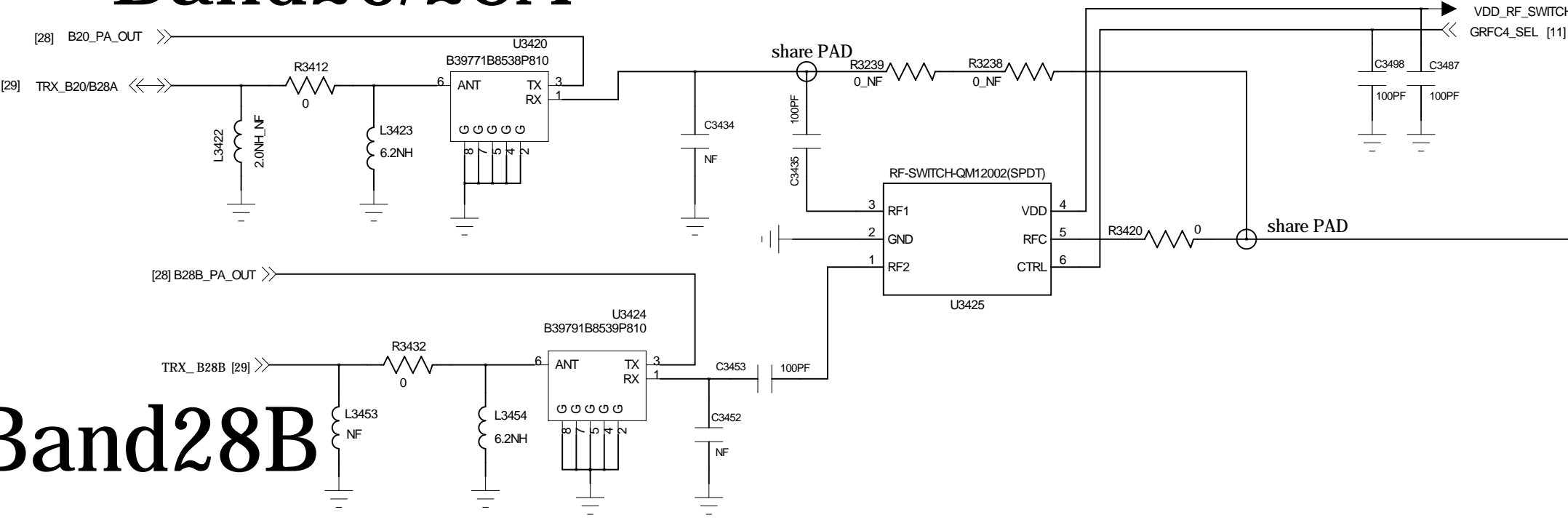
WTR0_PRX_LB2

Band3



WTR0_PRX_MB2

Band28B



Note:The matching need close to WTR, RX ports have DC at the pin, so it need DC block,

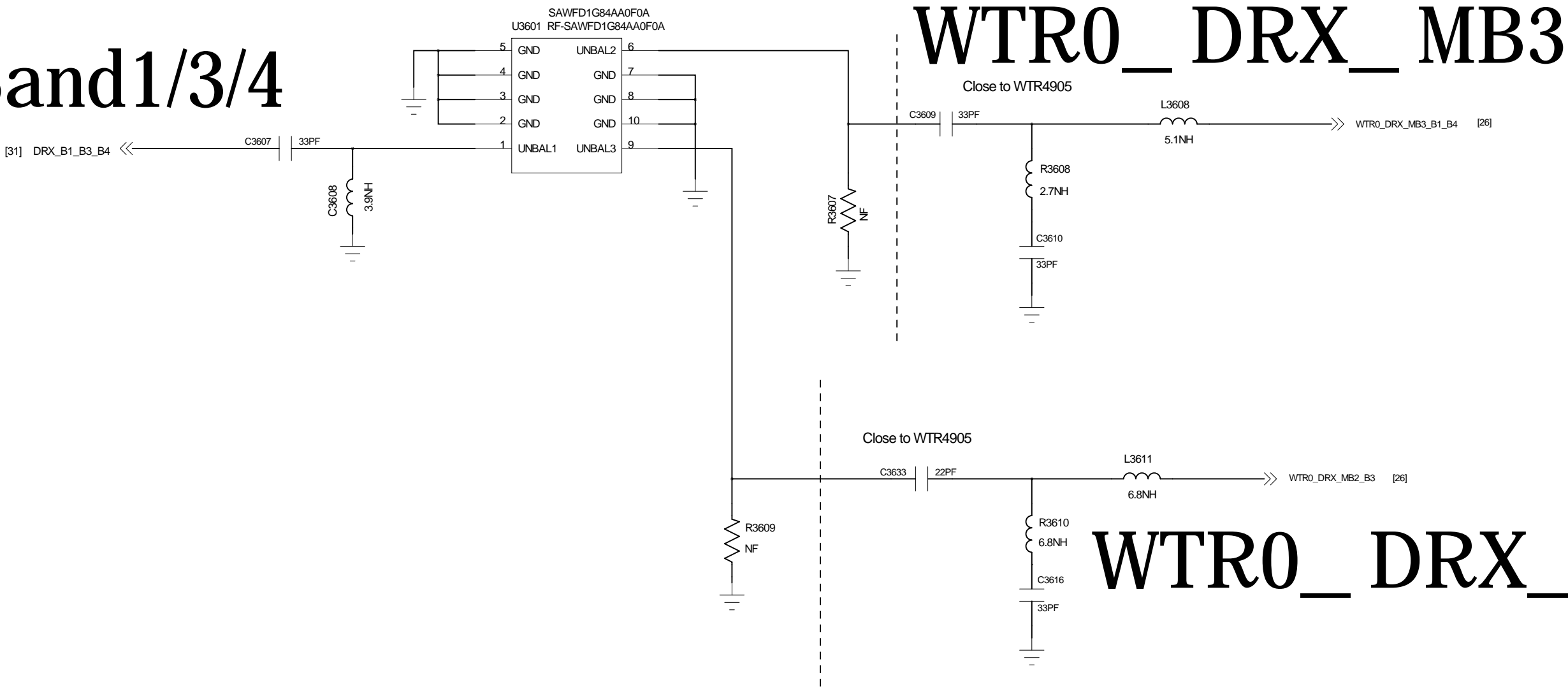
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Date:	Sheet	of

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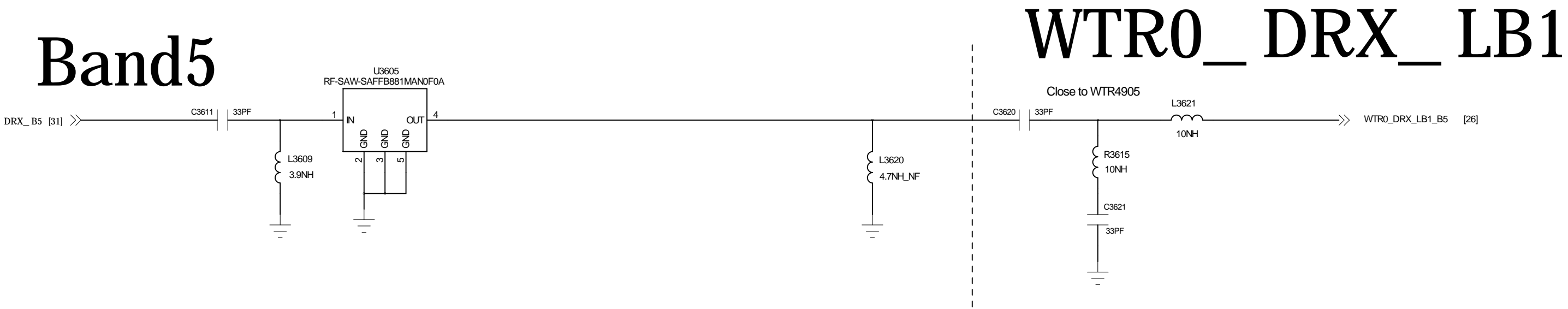


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Band1/3/4



Band5



Band20/B28



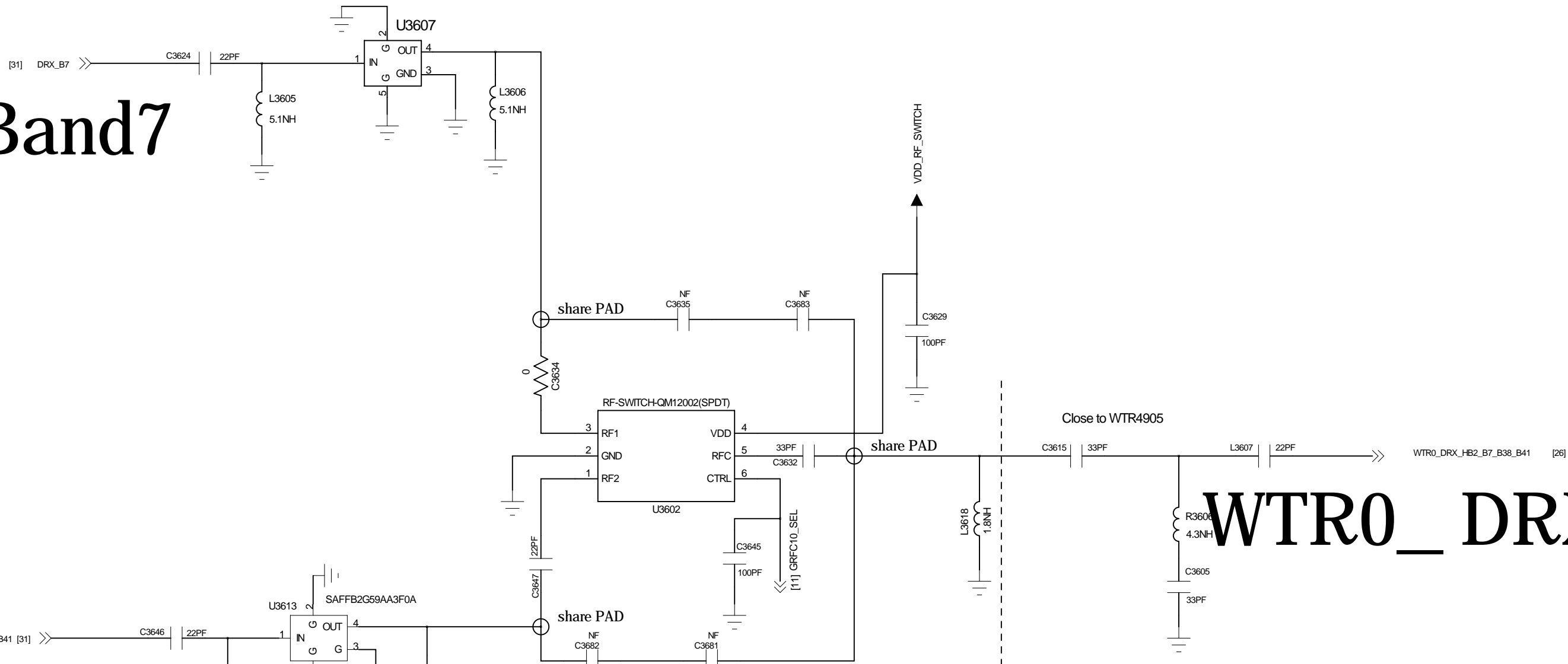
WTR0_DRX_LB3



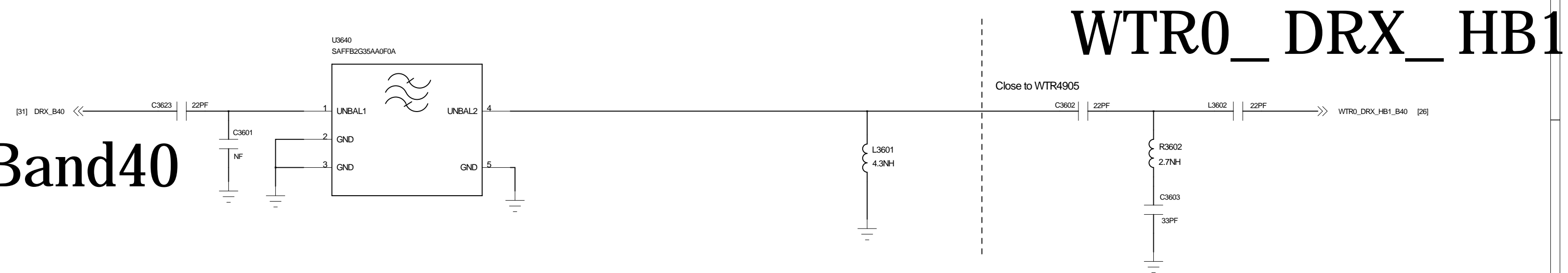
Band2



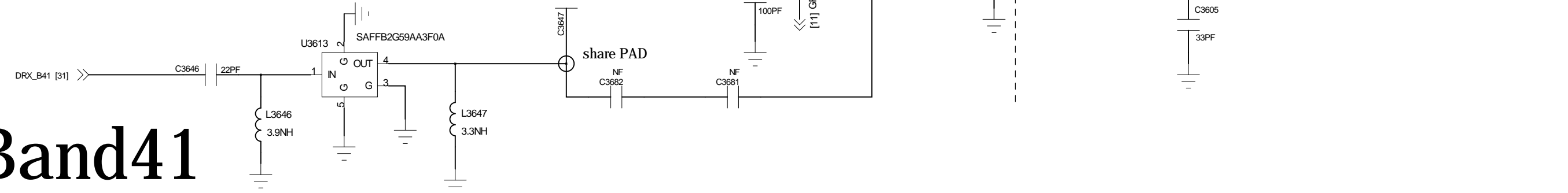
Band7



Band40



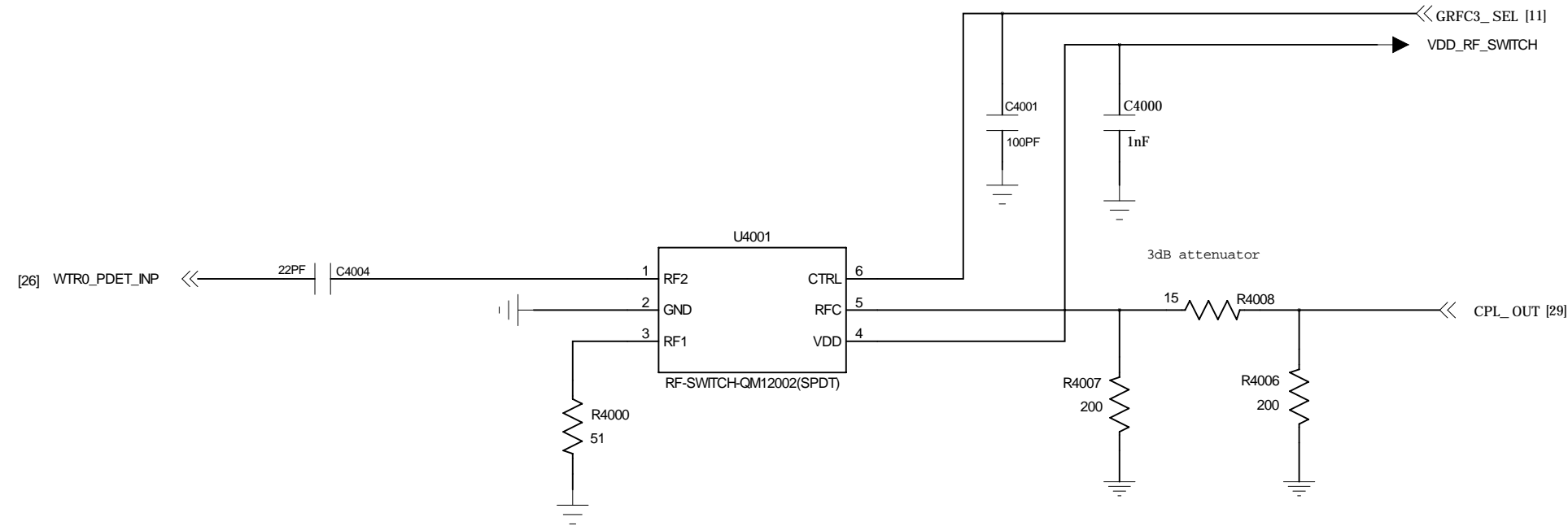
Band41



Note:The matching need
close to WTR, RX ports have
DC at the pin, so it need DC block,

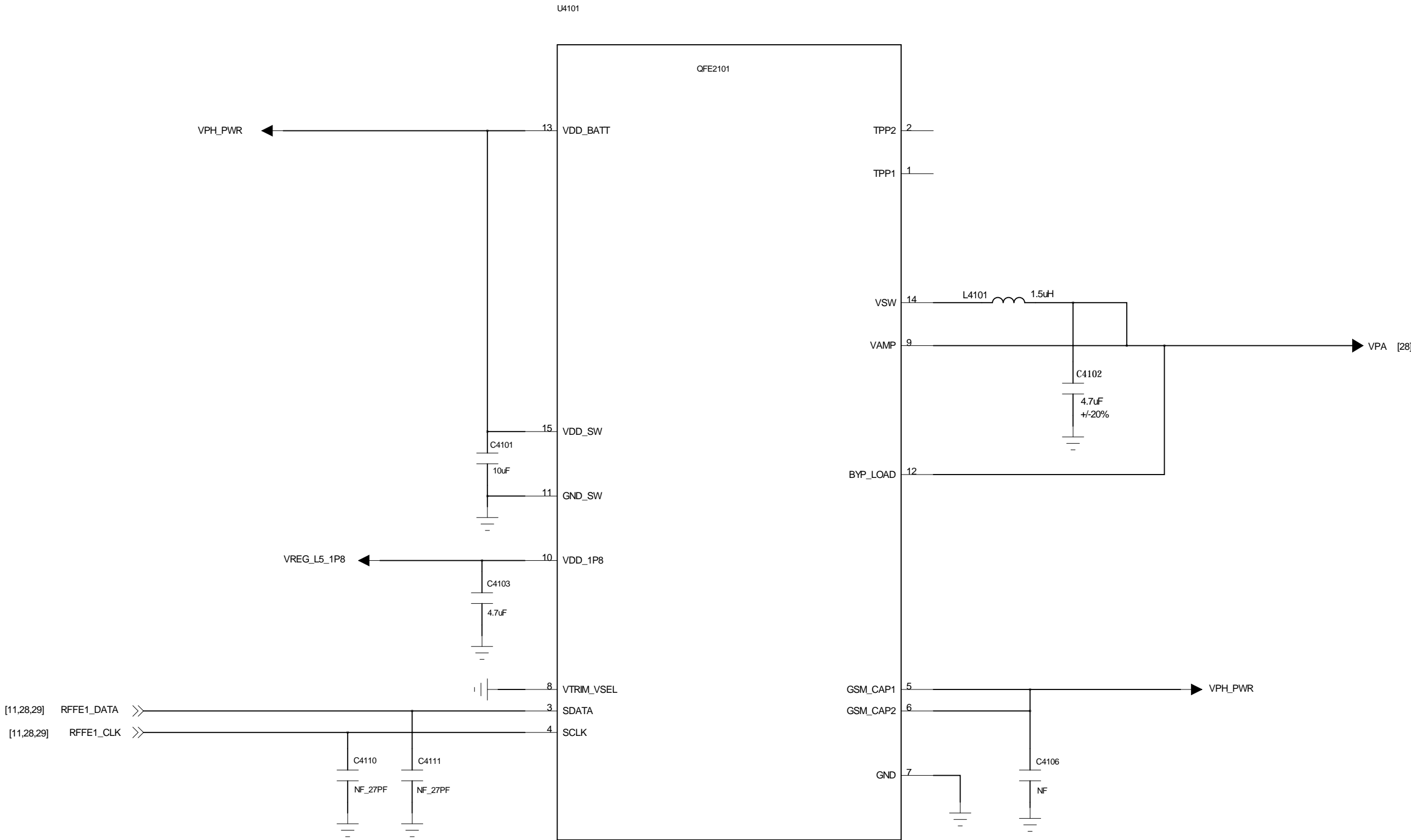
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SPDT

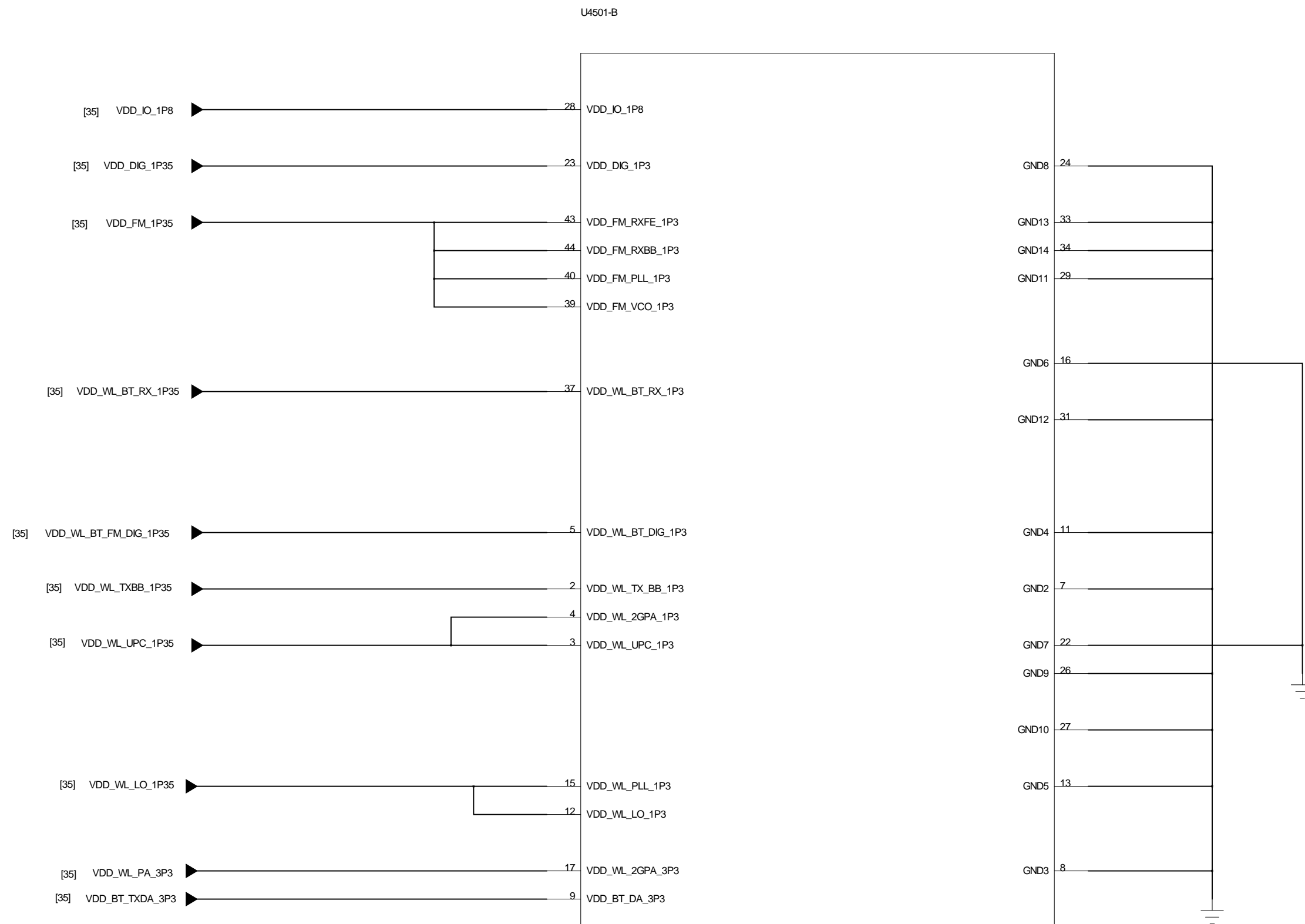
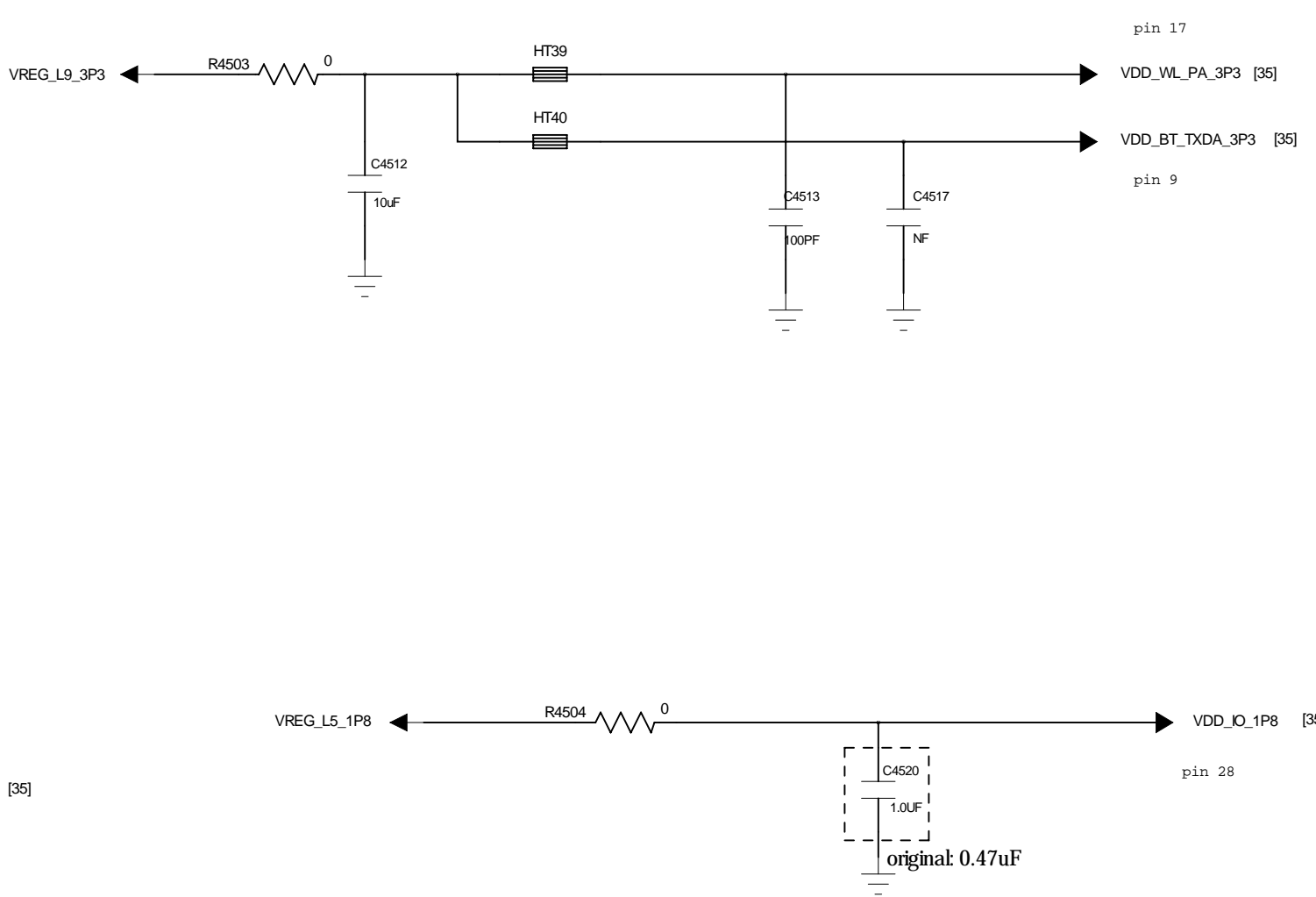
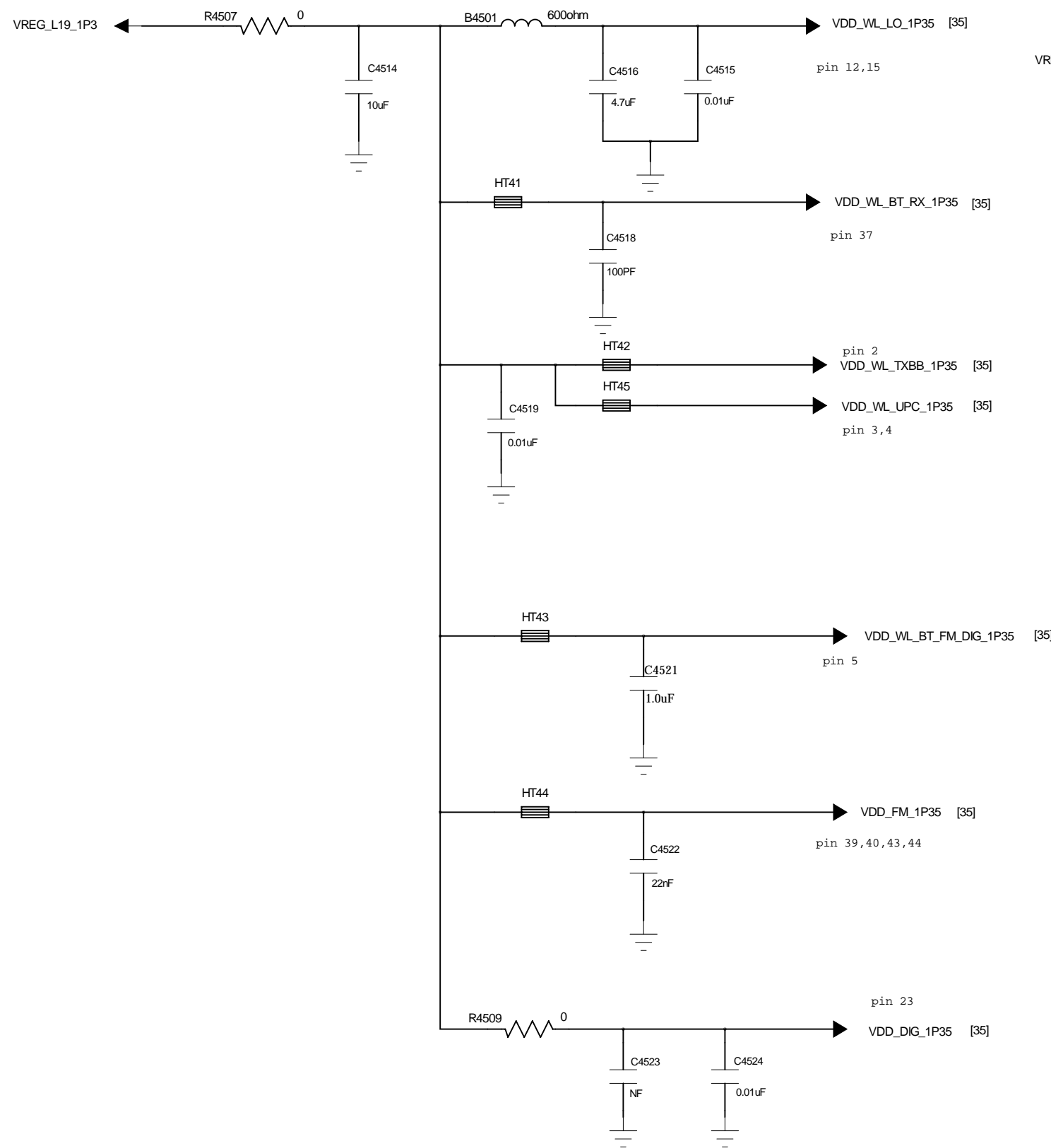
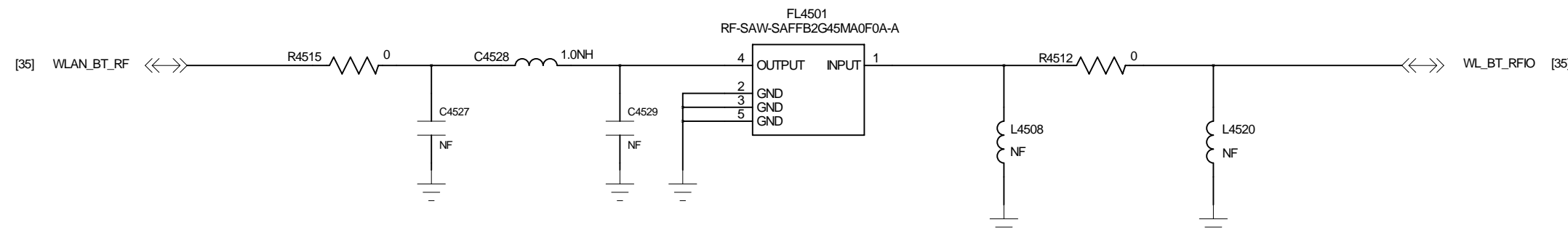
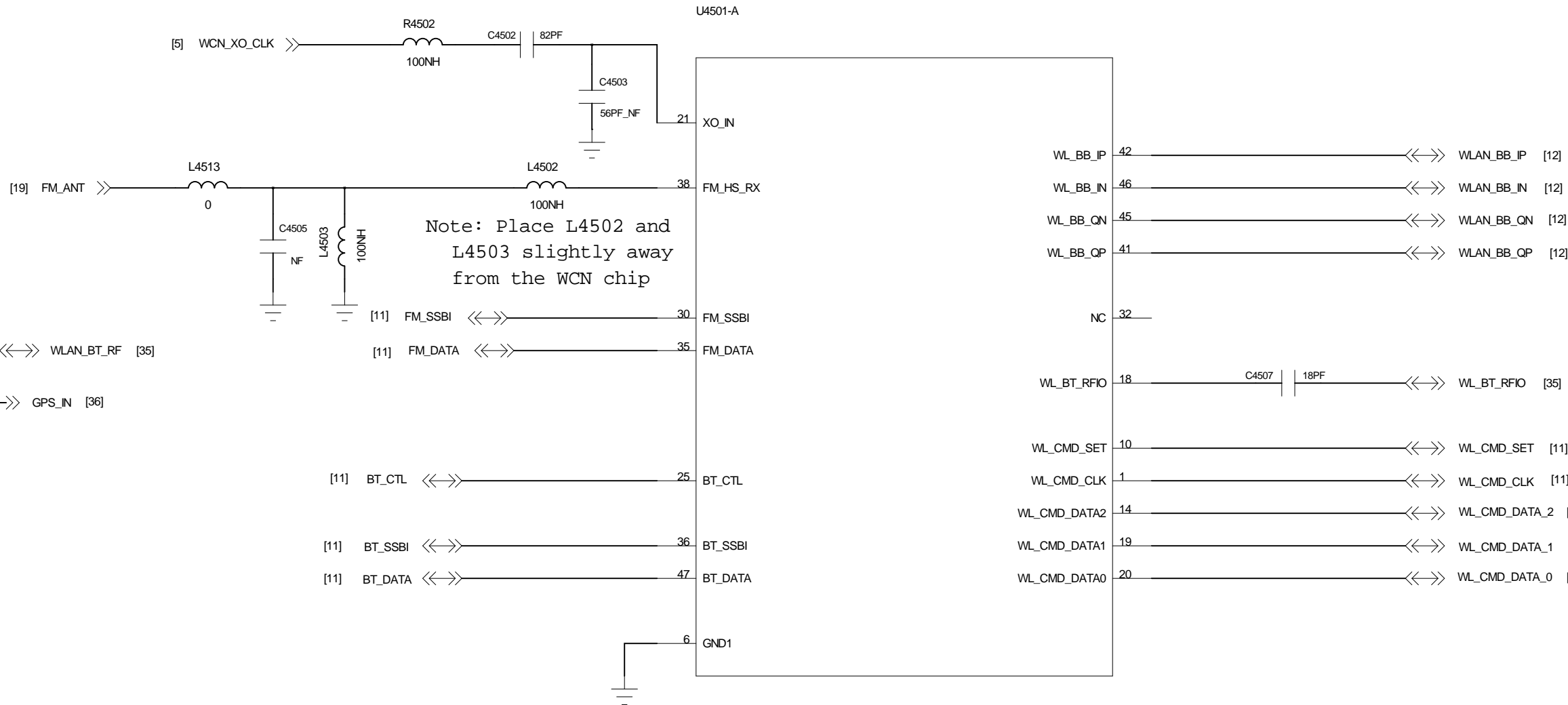
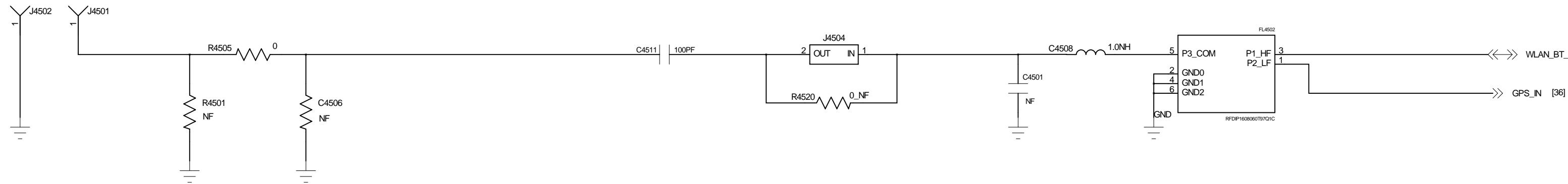


APT

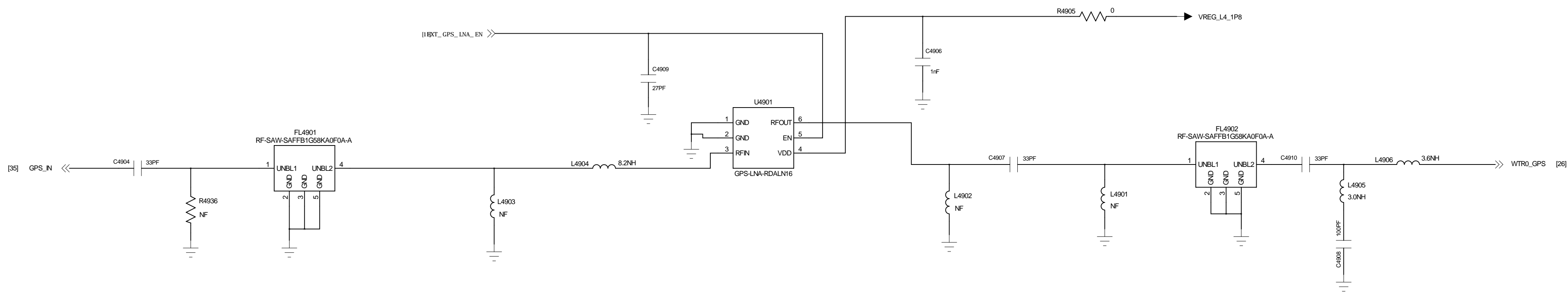
Note: Use a single low impedance power plane/fill VPA for all ET PA VCC1/VCC2.
Refer to 80-NA681-91 rev.B or later revisions for more layout details.



WCN3615



GPS



NFC

