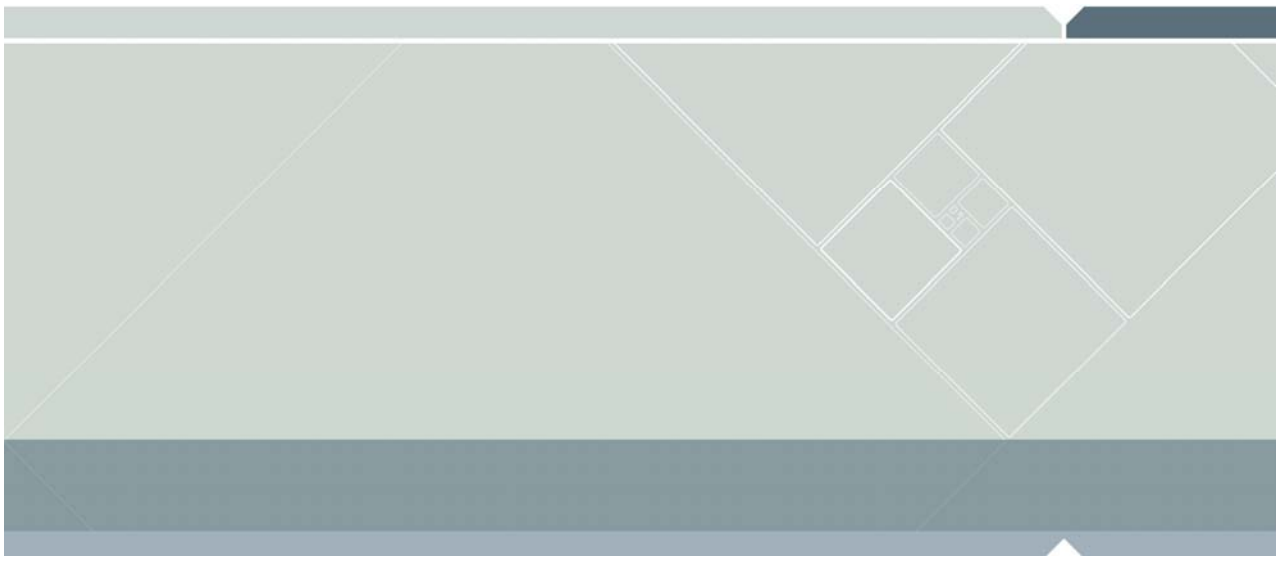

White Paper

MXC300-30 3G Mobile Platform Overview

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freescale™ semiconductor

Overview

Freescale's MXC architecture represents a radical simplification for smart wireless devices. MXC separates the two main domains of a cell phone: a modem core that communicates with the base station, and an applications core that powers the user experience. Because MXC cleanly separates these domains, designers can create new applications as quickly as they need to without touching the modem core. This reduces development costs and speeds time to market by as much as six months. An open operating system approach lets software developers deploy applications across a broad range of devices.

The MXC300-30 3G mobile platform, the first platform with a 3G single core modem, takes advantage of this architecture to reduce component count and cost. With MXC, OEMs and developers can create tiered solutions on one platform with features including advanced power saving techniques, integrated multimedia and OS-agnostic software.

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1 Introduction to the MXC300-30 Platform

Based on the revolutionary Mobile eXtreme Convergence (MXC) architecture, Freescale Semiconductor's MXC300-30 3G mobile platform provides a comprehensive solution that speeds time to market by simplifying development for manufacturers. By reducing component count and cost, the MXC300-30 platform enables consumers to have handsets that are slim, sleek and stylish. Integrated world-class power amplifier and power management technology helps reduce dropped calls and extend battery life. Highlights of the MXC300-30 platform include:

- Mature solution addressing upper low-tier and mid-tier 3G market segments
- Enables the lowest system cost for open operating system solutions
- Supports S60/Symbian, UIQ/Symbian, Windows Mobile® and Linux
- Low power solutions from a platform perspective, using sophisticated techniques such as dynamic voltage scaling, clock gating and low leakage process for maximum usage time
- Support and tools to reduce time to market and development costs

1.1 Single Core Modem

The MXC architecture distinguishes itself from most other cellular architectures with a single core modem. The single core processor at the heart of the MXC300-30 platform is a StarCore™ SC140e Digital Signal Processor (DSP) operating at up to 250 MHz. The single core modem handles the signaling protocol layers (Layer 1, Layer 2 and Layer 3) for 2.5G, 2.75G and 3G standards including GSM, GPRS, EDGE class 12 and WCDMA.

Applications processing technology is integrated into the chip with a shared memory system and shared peripherals. This eliminates the need for an additional external applications processor and helps to reduce cost. The modem and applications domains run on the same piece of silicon, which means more efficient interprocessor communication, higher performance, exceptional power management and reduced complexity.

Putting the entire communications stack on the DSP frees the applications processor, an ARM1136™ core operating at up to 532 MHz, to handle the operating system. The object of the single core modem architecture is to eliminate modem involvement in the ARM® processor on the same piece of silicon. This allows an open OS environment on the ARM side, without any entanglement from real-time tasks required for the modem.

Another advantage of this combined chip is the ability to use a shared memory structure. A separate modem and a separate applications processor can create additional expense associated with another set of DDR and ROM for the applications processor. The MXC architecture allows the applications processor and the modem to share the same piece of silicon and a single memory structure. Some of the caching structure in the MXC300-30 allows that memory resource to be reused in common without conflict between the modem and applications processor domains.

Learn More

Visit the websites for the MXC300-30 3G mobile platform and Freescale's MXC architecture, and download these PDF-format white papers:

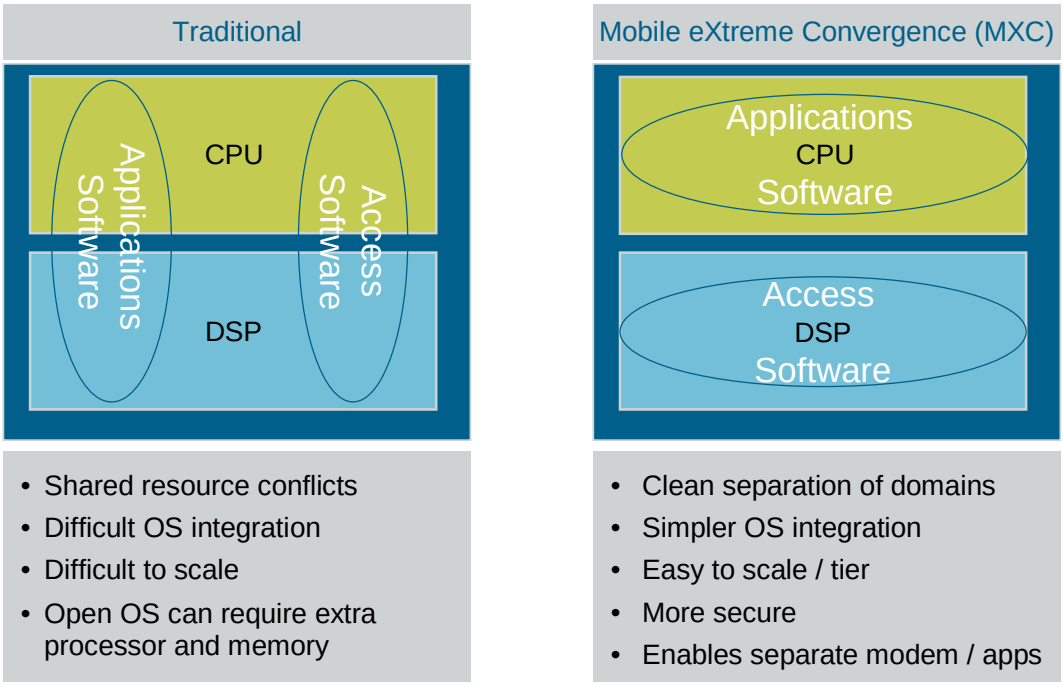
- Integrating Operating Systems with Freescale's Cellular Software Platform
- A Streamlined Architecture to Deliver Mass-Market Mobile Converged Devices
- Reducing Time to Market: Parallel Software Development with Emulation and Simulation Tools for MXC Architectures

1.2 MXC Value Proposition

Traditional architecture in the RTOS world generally means intermixing the Layer 2 and Layer 3 signaling on the ARM processor side, and having a DSP dedicated to the Layer 1 stack. In the open OS world, eliminating Layer 2 and Layer 3 of the cellular modem stack from the applications processor domain and keeping it restricted to the DSP greatly simplifies operations on the applications processor side. (A designer could always choose to add another ARM processor, such as an ARM9™, to facilitate the Layer 2 and Layer 3 processing.)

Using the restricted memory spaces and the different modes within the StarCore DSP and the ARM processor also helps security. Given the trend towards open architectures and operating systems, users can install software and functionality on the handset. The easier it is to install applications on a device, the easier it is to attack the security of the device. The MXC300-30 platform uses both hardware and software to enable key security features. By helping to ensure that applications are not able to encroach into the communications space, the architecture can protect against intentional tampering with communication processing as well as accidental downloading of viruses.

Figure 1.1. Traditional vs. MXC Architecture



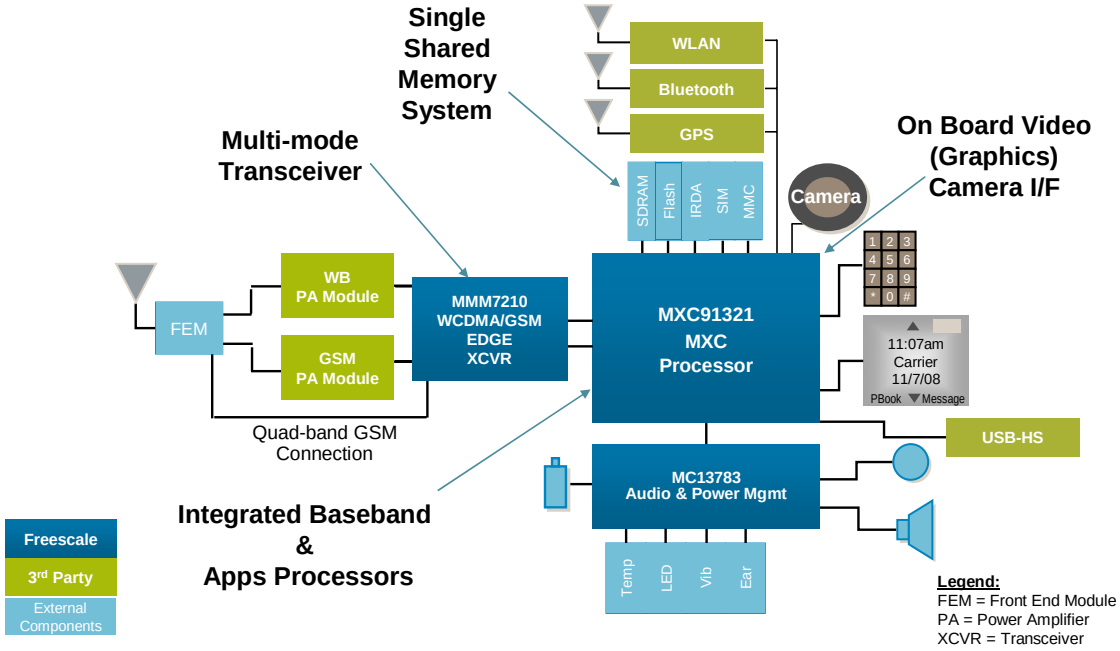
1.3 MXC300-30.2 Reference Design

The first version of Freescale's 3.5G smartphone solution, the MXC300-30.1 reference design, is a comprehensive solution for 3.6 Mbps HSDPA smartphones featuring Symbian OS™ and S60 software. Symbian OS and S60 are integrated and pre-validated, including S60 recommended system tests, to minimize development time and cost and maximize system stability and maturity. Pre-validated network capabilities such as GCF, IOT and field testing help shorten time to market for phone manufacturers.

The MXC300-30.2 reference design builds on the first version with a multimode single-chip transceiver that handles both WCDMA and GSM on the same piece of silicon. The MMM7210 transceiver is a highly integrated transceiver that combines quad-band GSM/EDGE functions with up to four WCDMA bands in a single package solution. The receiver has five inputs supporting both WCDMA and GSM/EDGE and uses a new RF front-end topology for superior intercept points. The receiver also includes anti-aliasing filters, digital channel filters, digital gain control and high dynamic range ADCs. This transceiver cuts the part count for phones built with the MXC300-30.2 reference design, saving both cost and valuable board space.

The MXC300-30.2 reference design also features the MC13783, a highly integrated power management, audio and user interface component dedicated to handset and portable applications covering GSM, GPRS, EDGE and UMTS standards. This device implements high-performance audio functions suited to high-end applications, such as smartphones and UMTS handsets. The reference design also features wide peripheral support capability including Bluetooth, GPS and WLAN.

Figure 1.2. MXC300-30.2 Reference Design



2 MXC300-30 Hardware

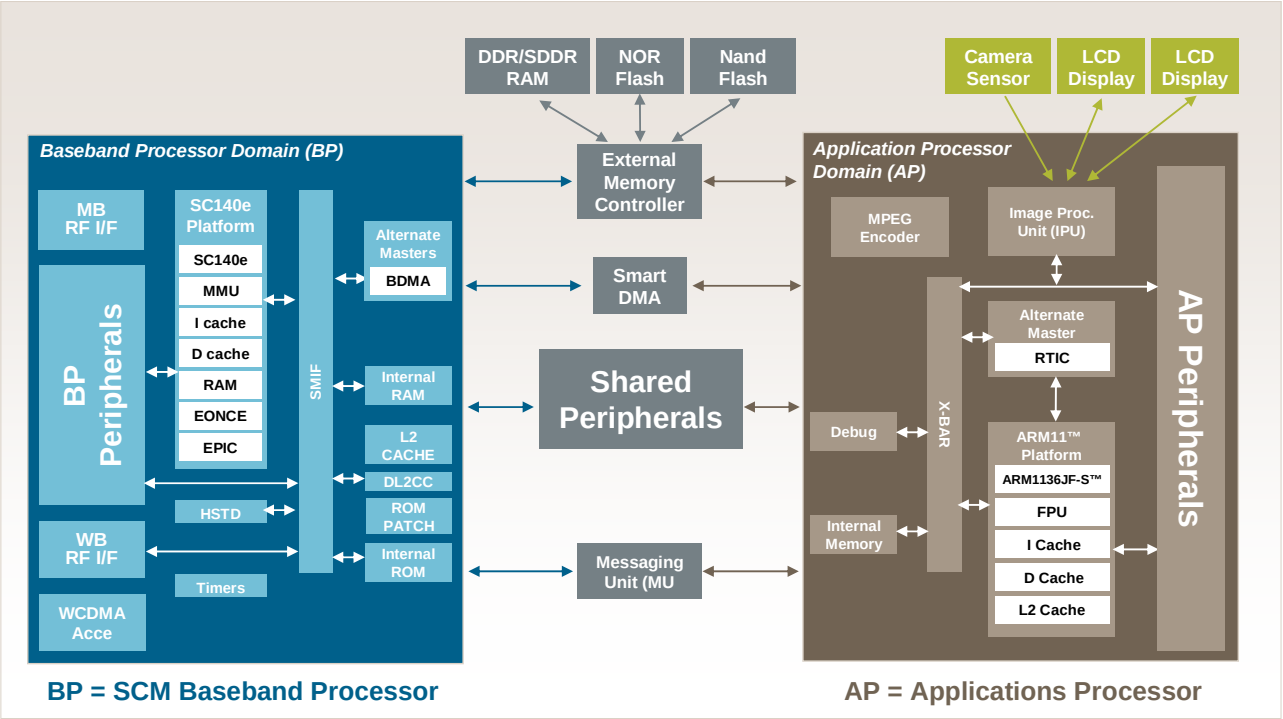
MXC hardware architecture, with its ability to consolidate important modem functions on the StarCore DSP and innovative technology to allow both processor cores to share a single external memory part, creates a uniquely cost-effective hardware solution for 3G cellular phones.

The heart of the MXC300-30 platform is the MXC91321 processor, which contains the baseband and applications processors. A memory messaging unit is used for setting up communication. Certain shared peripherals, such as USB, between the baseband processor and applications processor can be assigned to either the applications processor or the baseband side of the domain. From a software perspective, it is easier to assign a shared peripheral exclusively to one side or the other. A smart DMA controller can be used for some of the message processing between the baseband and applications processors domains. MXC software uses part of this; primarily it uses the shared common memory structure which controls DDR, SDRAM, NOR Flash or NAND Flash. The complete hardware and software platform has NAND shadowed to DDR memory. DDR is usually needed for high speeds. While execute-in-place on NOR Flash is not used as much as it once was, NOR Flash does not need to wait for a download to DDR every time software is debugged. Many newer handsets use the technique of shadowing NAND to DDR.

The StarCore 140e baseband processor is a DSP with a high-speed turbo decoder for UMTS decoding. A chip rate processor has an interface to the MMM7210 transceiver. The MXC design puts some of the routines that are very mature in the Layer 1 stack in internal ROM. From a power consumption and speed perspective, anything on the M1 bus for the processor operates at processor bus speeds, so it's very fast. The disadvantage of putting it on that bus directly is the amount of loading on the bus. ROM has less loading than RAM, so more ROM is preferable. While ROM has certain disadvantages in terms of the software, it has the advantage of better power consumption on the DSP side. This processor has an L2 cache structure. The partition can be moved around on the L2 cache and M2 memory, essentially locking sections of the cache in so that it becomes M2 memory within the processor.

The applications processor side runs on a Java-accelerated ARM1136 processor with a floating point unit and Layer 1 and Layer 2 caches. Multimedia support includes an MPEG encoder hardware accelerator and an image processor interface for camera and both primary and secondary LCD support.

Figure 2.1. MXC91321 MXC Processor



2.1 Modem Domain

The baseband achieves 3.6 Mbps HSDPA at 312 MHz on the four-MAC DSP. Because HSDPA is bursty by nature, peak DSP load varies. This requires high peak performance, but in a low power and area implementation. To provide this, Freescale's solution has a turbo mode in the DSP. This turbo mode increases DSP core frequency (and voltage) to increase DSP performance for the short period of the peak load. To reduce power consumption, the turbo mode uses dynamic voltage and frequency scaling to reduce DSP core frequency and voltage outside of these peaks. This helps reduce power consumption and costs.

At the circuit level, the MXC architecture applies best-in-class design practices to obtain the lowest standby power for long battery life. The C90 process for this chipset uses well biasing, which is a negative generator on the substrate that automatically goes to deep sleep mode. Advanced techniques such as dynamic voltage scaling (DVS) are also used to achieve power savings, particularly for tasks such as voice calls where high speed operation is not necessary. Extensive use of clock gating also conserves power.

The MXC300-30 baseband supports advanced equalization and diversity. For the baseband, implementing diversity for WCDMA is a relatively easy task. This part essentially has seven fingers for the rake which can be divided in any ratio between the primary and diversity ports associated with it.

Cell phone manufacturers often have their own rendition of the modem stack. However, in the future, manufacturers will want to focus on value-added features—what distinguishes them from the competition. It is likely that more semiconductor companies will provide the software stack for Layers 1, 2 and 3. Many manufacturers already use ARM processors for Layers 2 and 3.

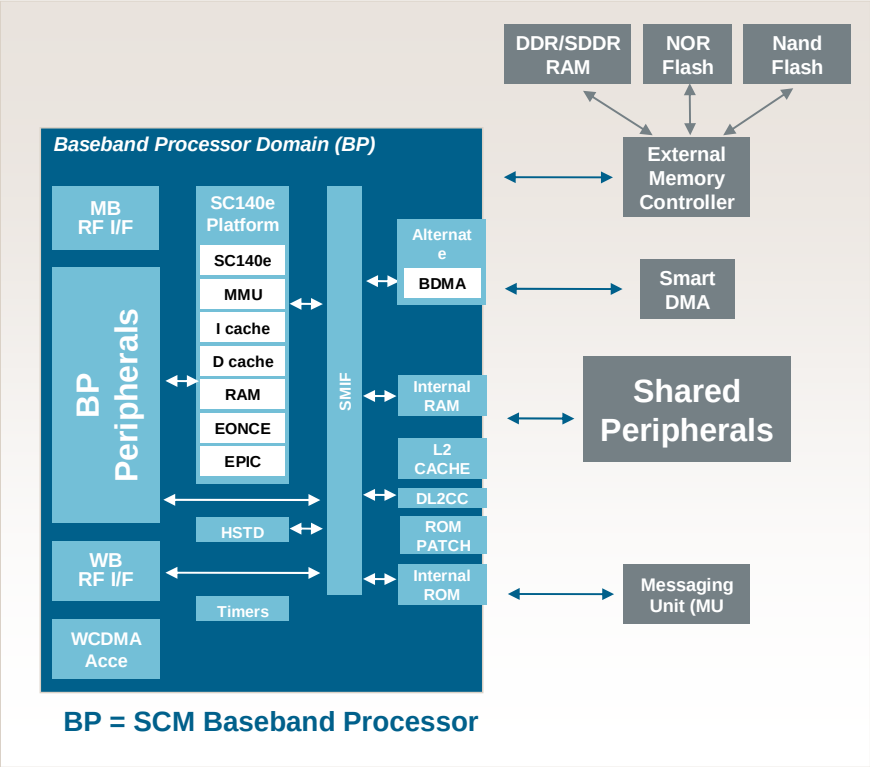
Key technical features of the MXC300-30 baseband include:

- StarCore SC140e DSP
  - 250 MHz maximum frequency for 1.8 Mbps HSDPA
  - Upgrade to 312 MHz for 3.6 Mbps HSDPA

- L1 caches: 16KB I, 32KB D
- L2 cache: 128KB

- 4-ALU VLIW architecture
  - 6 Instructions fetched/cycle
  - Variable length execution set
  - 1000 MMAC @ 250MHz
  - 1500 MIP @ 250MHz
- MMU, task protection, security
- Modem hardware accelerators
  - WCDMA: Searcher, demodulator, transmitter, turbo decoder
  - Ciphering
- Advanced power management
  - DVFS, well biasing, clock gating

Figure 2.2. Baseband Domain in the MXC91321 MXC Processor



2.2 Applications Processor Domain

As in the DSP domain, the ARM11™ applications processor has L1 and L2 cache. The two L2 caches together from the DSP and applications processor domains greatly facilitate the use of the shared memory structure. Although this technique is not necessary, it helps decouple the DSP from the ARM as far as external memory is concerned.

Integrated video graphics mean that the system does not need an external graphics processor. With the integrated image processing unit (IPU) the MXC300-30 can run a 2- or 3-megapixel camera. The current platform recommends a

JPEG compressor in the camera at 3 megapixels and above. A JPEG4 encoder helps JPEG4 hardware acceleration, particularly for the encoding function which requires more MIPS than the decoding function. Shared memory interface and smart DMA engine help the communication between the DSP and applications processor sides.

Key features of the applications processor domain include:

ARM11 core

- ARM1136™ 8-stage pipeline
- Branch prediction
- MMU task protection, security
- Floating point, Java™ hardware support
- L1, L2 caches
- 400 MHz (nominal) at 1.2 volts, 532 MHz (turbo mode) at 1.6 volts
- Advanced power management

Imaging/video subsystem

- Image processing unit (IPU)
  - Camera and display interfaces
  - Display buffer
  - Rotation, scaling, pre/post
- MPEG4 encoder

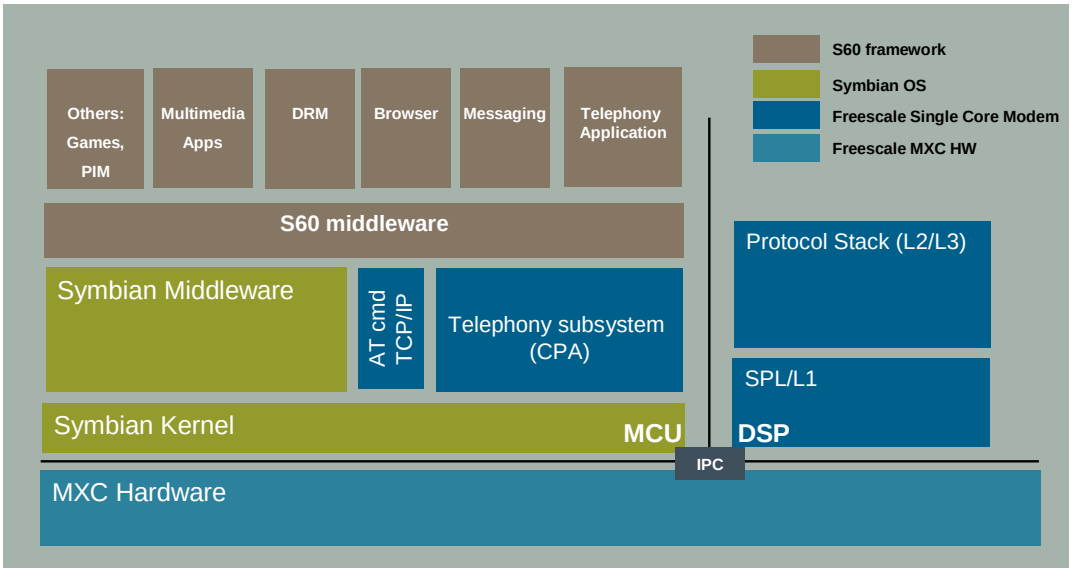
Shared memory subsystem

- Shared memory interface
- Smart DMA engine
- Messaging unit

3 MXC300-30 Software

Layers 2 and 3 of the protocol stack are executed on the StarCore 140 as is the L1 cache in conjunction with the previously mentioned hardware accelerators, the chip rate processor and the high speed turbo decoder. Figure 3.1 shows a Symbian rendition with the S60 middleware. The middleware, of which Freescale supplies a piece and Symbian supplies a piece, could be an AT command set in a particular rendition. Middleware is in the Symbian and Series 60 environment, then the various application layers are at the top.

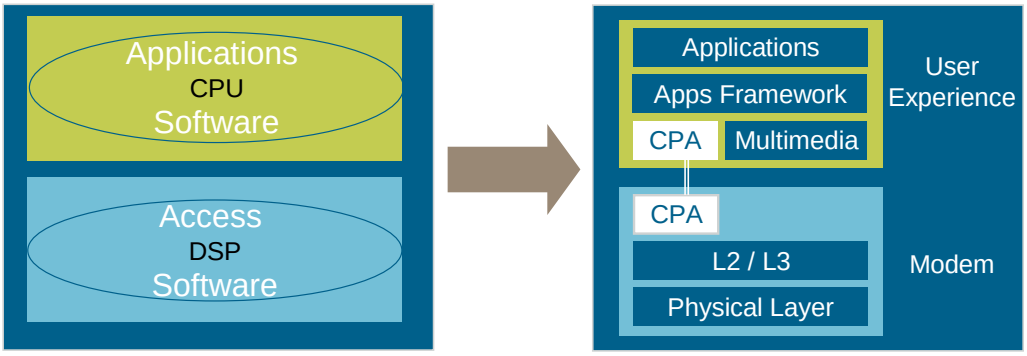
Figure 3.1. MXC300-30 Software using a Symbian and S60 Example



3.1 Cellular Platform Access (CPA)

Freescale's Cellular Platform Access (CPA) software decouples the modem from the operating system and applications. CPA helps manage the common memory space and essentially replaces the older AT command set environment with a structure that allows the modem to communicate with the application layer in a relatively controlled manner that is OS-agnostic. The CPA software architecture helps OEMs bring powerful handsets to market quickly with the flexibility to tailor the handsets to their individual business strategies.

Figure 3.2. CPA Software Architecture



CPA is designed to be a reusable, OS-independent interface to adapt a cellular platform to different operating systems. CPA can take advantage of unique technical benefits in the MXC cellular platform, including clean separation of the communications and applications stacks, for faster and less expensive software development and more efficient approaches to 3G standards.

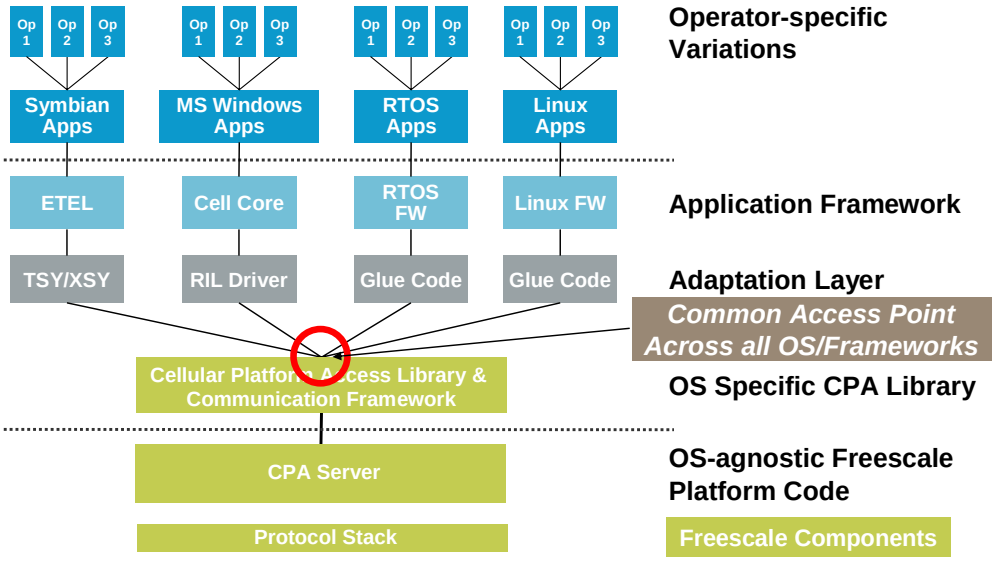
The objective in developing CPA was to examine various operating systems and discover a commonality in order to arrive at a common CPA interface that minimizes uniqueness from OS to OS. Each operating system has its own adaptation layer, a minimal section of code that goes on top of CPA. Once the modem is validated and stable, other operating systems and frameworks on can be ported on top of CPA. This leads to faster implementations of other operating systems. The first OS to go through validation was MXC300-30 with Symbian and S60.

One notable feature of the MXC hardware architecture is that it consolidates the real-time sensitive network communications software on the StarCore DSP. This hardware/software partitioning provides several benefits. Most

open operating systems cannot support the very low latencies that the 3GPP air-interface standards require. Even if open operating systems could support the timing requirements, they still would require significant porting and retesting. The MXC architecture allows one external random access memory to contain code and data for both the application and baseband processor, resulting in reduced part count, more efficient memory use and overall lower handset bill of materials.

By consolidating the entire 3GPP protocol stack on a single processor, the MXC architecture eliminates the need to port that software to each operating system environment. To further enhance software reuse between operating system platforms, the CPA architecture divides the problem of adapting the modem software to the operating system and application framework into two parts: the CPA component, which is OS-independent and highly portable, and the OS adaptation layer.

Figure 3.3. Cellular Platform Access (CPA) Software Structure



3.2 Advantages of MXC Software Architecture

MXC software drives reductions in system size and cost. Having the modem and applications processors in a single chip eliminates the need for a separate applications processor to support mobility management functions. The single platform memory system saves the cost of the external part count associated with two memory subsystems. Integrated video and graphics processing also saves part count and board space by eliminating the need for an external graphics processor. And the MXC300-30 platform is built upon a proven, stable 3G protocol stack.

The demand for open operating systems is being driven by the need for a true application development platform that benefits both operators, who want to keep adding features at low cost, and end users who demand more productivity and value from those features. Network bandwidth is increasing as 3G becomes ubiquitous, while decreasing hardware costs are making phones based on open operating systems more cost-competitive with traditional RTOS phones. MXC's independent application and modem environments facilitate open operating systems and the ability to select multiple operating systems on the same hardware platform.

The standardized CPA interface among MXC platforms allows portability among Freescale platforms, while the MXC architecture allows the most efficient use of memory and components. This architecture will be carried forward in next-generation MXC platform nodes, allowing customers to reuse their software investments.

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